# SPEAKER

## 4th Panel Level Packaging Symposium
## SEPTEMBER 8, 2022 | BERLIN

**Rolf.Aschenbrenner @izm.fraunhofer.de**

**Rolf Aschenbrenner** has worked from 1991 to 1992 at the University of Gießen and in 1993, he joined the Research Center for Microperipheric Technologies at the Technical University of Berlin. Since March 1994 he has been employed at the Fraunhofer IZM in Berlin where he is presently the Deputy Director and Head of the Department System Integration and Interconnection Technologies. He received the iNEMI International Recognition Award in 2005, the CPMT David Feldman Outstanding Contribution Award 2013 and the European Semi Award 2016. He served as IEEE EPS Vice President, Technical and IEEE EPS Vice President, Conferences. From January 2010 until December 2011 he was IEEE EPS President and in 2012 he became IEEE Fellow.

**Tanja.Braun @izm.fraunhofer.de**

**Tanja Braun** is head of the group Assembly & Encapsulation Technologies. Recent research is focused on fan-out wafer and panel level packaging technologies and Tanja Braun is leading the Fan-out Panel Level Packaging Consortium at Fraunhofer IZM Berlin. Results of her research concerning packaging for advanced packages have been presented at multiple international conferences. She holds also several patents in the field of advanced packaging. In 2014 she received the Fraunhofer IZM research award and in 2021 the Exceptional Technical Achievement Award from IEEE Electronics Packaging Society (EPS) and the IMAPS Sidney J. Stein Award. Tanja Braun is an active member of IEEE. She is member of the IEEE EPS Board of Governor (BOG) and the IEEE EPS Region 8 Program Director.

**Eoin.OToole@ amkor.com**

**Eoin Otoole** is a the Technology Development Director in the Package Development department of Amkor Technology Portugal.

Originally from Dublin Ireland where he obtained his primary and master degrees in material science from Trinity College Dublin.

He has 25 years of experience in semiconductor pacakage development and manufacturing.

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sylvester.demmel
@asmpt.com

**Sylvester Demmel** holds the position as Senior Product Manager for SIPLACE Advanced Packing with ASMPT in Munich Germany. ASMPT is a leading supplier of packing equipment and SMT placement machines. He has over 30 years of experience in the electronic manufacturing industry, since 2008 specialized in advanced packing and has lived and worked in North America and Europe. Sylvester Demmel began his career with Siemens in 1990 and has held various managerial positions abroad and in Europe and was responsible for the Chip Assembly business within Siemens. He is currently based in Munich Germany. Sylvester Demmel completed his studies with a Mechatronics degree from the University of Applied Sciences in Munich, Germany and holds several patents.

Lars.Boettcher
@izm.fraunhofer.de

**Lars Boettcher** is an R&D engineer and project manager at Fraunhofer IZM in Berlin, were he leads the group "Embedding and Substrate Technologies". He has worked in the Department for System Integration and Interconnection Technologies for 22 years, and he specializes in packaging process development with emphasis on printed circuit board manufacturing technologies. He is responsible for different projects with industrial partners, as well as German and European Union funded projects, which focus on new package technologies based on embedded chips and new substrate technologies. Recent projects focus on technologies for power electronics applications, based on component embedding, as well as on panel-level packaging aiming for ultra-fine line and pitch technologies.

m.Leitgeb
@ats.net

**Markus Leitgeb** is the Manager of the Group R&D Center Austria of AT&S. His team is responsible for the development of new platforms for High Performance Computing, High Speed/Frequency and Power Efficiency. Markus has joined AT&S in December 2000 was leading the team to develop alternative concepts for flexible interconnections and Cavities, which were rolled out to plants in Austria and China. Markus holds more than 100 active patents and has published several papers in the field of PCBs (2014 IPC APEX EXPO Best International Paper Award). He is an active member in iNEMI and in the Packaging Technologies subcommittee of ECTC. Markus holds a M.Sc. in Polymer Engineering from the University of Leoben, Austria.

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roland.rettenmeier
@evatecnet.com

**Roland Rettenmeier** has worked in the field of Electronics and Semiconductor manufacturing since 2001, managing multiple international projects. After joining Evatec in 2016 as Senior Product Marketing Manager (PMM) within the Business Unit for Advanced Packaging, he focused on business development for Panel Level Packaging where Evatec has now become the recognised market leader for thin film technology solutions. Since 2020 he has also supported development of Evatec's wafer level packaging solutions business. In addition to his market and customer responsibilities, Roland represents Evatec in the Panel Level Packaging consortium of Fraunhofer IZM Berlin, in the Packaging Research Center at Georgia Tech, USA and in the Panel Level Packaging Consortium at the NCAP in Wuxi, China.

sanjay.malik
@fujifilm.com

**Sanjay Malik** is a highly skilled Senior Executive Technology Leader at Fujifilm Electronic Materials with extensive experience in developing and commercializing innovative materials in the diverse areas of semiconductors, pharmaceuticals, coatings and petrochemicals.

He combines empathy and a passion for people, with superior skills in project management, group leadership, and building strategic alliances. He was working on more than 90 issued patents.

mathilde.billaud
@izm.fraunhofer.de

**Mathilde Billaud** is a research Fellow at Fraunhofer IZM since 2017. She is now involved in an industrial Consortium organized by Fraunhofer IZM, on Fan-Out Panel Level Packaging to model the complete process flows related to the different technology options for chips packaging on panel developed in Fraunhofer IZM. The modeling enables a combined cost and environmental assessment. This methodology is now transferred to other research and industrial projects. Her favorite research topics cover critical materials, resource and energy consumption, as well as circular practices in microelectronic manufacturing. She received a doctor's degree in 2017 for her thesis "integration of III-V materials as high mobility channel for MOSFET transistor".

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**gabriela.pereira@yolegroup.com**

**Gabriela Pereira** is a technology and market analyst working in the advanced packaging team within the Semiconductor, Memory and Computing Division at Yole. Gabriela focuses on advanced packaging platforms, develops technology & market reports, and is engaged in dedicated custom projects. Gabriela's experience in the semiconductor field includes working at Amkor Technology, first for her master's thesis and then as a R&D Engineer, where she collaborated on several package development projects. Gabriela holds a master's degree in Metallurgical and Materials Engineering from the University of Porto, Portugal.

**tarek.a.ibrahim@intel.com**

**Tarek Ibrahim** is an Intel Senior Principal Engineer who joined Intel Oregon, in 2004 as a Si Integration Engineer and developed the Metal Interconnect patterning processes for 45nm and 22nm process nodes. In 2011, he joined Intel Arizona as Package Integration Engineer and worked on the panel-level die embedding program. In 2013, he became the TD Integration Manager leading the team who certified the Chandler Substrate Factory and developed the EMIB process. In 2018, he moved to lead the Package pathfinding efforts with focus on Substrate PF Roadmap to enable the Package Architectures needed across the Intel product segments. He is currently leading a small team of Technical Program Managers to develop the next generation of Disruptive Substrate Packaging Technologies and building blocks.