Fraunhofer IZM

Fraunhofer Institute for Reliability and Microintegration IZM

Hardware Protection in the Age of Modern Microelectronics

Chiplet approach for 77 GHz MIMO radar

Research Project VE-REWAL

RDL-1st substrate wafer with assembled chiplets

Microelectronics are already an integral part of our everyday lives and are set to take over an even more important place with the advent of self-driving vehicles and service robots. The electronic systems required for this must not only meet stringent requirements in terms of costs, performance, reliability, miniaturization, or sustainability. They must also be trustworthy.

However, criminal attempts at manipulating such systems cannot be ruled out in the industrial production of complex electronic systems. Possible inroads for tampering or corruption include unauthorized interventions such as the replacement of components.

New methods, solutions, and processes have to be found to prevent tampering along the entire value chain. Fraunhofer IZM is refining the process of fan-out wafer-level packaging (FOWLP) to enable true control over each individual component.

As part of the BMBF project VE-REWAL »Know-how Protection for Trustworthy Heterogeneous Electronic Systems with Chiplets«, a sample 77 GHz MIMO radar for driver assistance systems will be used to demonstrate how technology of this nature can be kept trustworthy and reliable.

Fraunhofer IZM is contributing to the VE-REWAL subproject »Redistribution layer (RDL)-1st for Trusted Chiplet Packaging«. In order to protect RF chiplets for the radar system against manipulation and to equip them with a trust architecture, the functions of the electronic system are obfuscated by a novel system partitioning and system packaging approach. The chiplets will be realized for radar ICs and investigated at the FOWLP and board level as well as in actual application.

Innovations to be realized:

- Further development of the wafer level packaging technology to realize trusted heterogeneous systems with RF chiplets and complex signal processing in a single package.

Coordinator

- University of Bremen

Project partners

- Conti Temic microelectronic GmbH
- Infineon Technologies AG
- Fraunhofer IZM
- Fraunhofer FHR
- Ruhr University Bochum
- Technical University Ingolstadt
- Viconnis (associated partner)
- PHYSEC GmbH (associated partner)

Project volumen

- € 6 million
- 86 % Funding share

Duration & Funding code

- 05/2021 - 04/2024
- 16ME0308

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Velektronik

Contributions of Fraunhofer IZM:

- Conceptual development for combined HF/HD chiplets
- Defining the specifications and boundary conditions for HF-RDL
- Developing the specific process for HF/HD RDL substrates
- Fabricating a HF/HD FOWLP chiplet technology demonstrator
- Comparing different technology approaches (eWLB vs. RDL-1st FOWLP)
- Producing a functional demonstrator for HF/HD chiplets

Distributed algorithms, split manufacturing (production of different parts by different manufacturers), and functional changes to the program code are used to protect the electronic components against tampering.

The encryption of data traffic between the components using additional smart cards is another safety-critical aspect. To conceal the functionality, layout, and intellectual property from third parties, the signal processing of individual chips is distributed over several chiplets. Gaining access to individual chiplets would thus be rendered worthless for attackers.

Advantages of distributed functions on chiplets:

- IP protection for the overall system
- Simultaneous cooperation with different suppliers

To provide reference data for future industrial manufacturing, the RF/HD FOWLP concept will be realized on a 300 mm BEOL wafer line. This will also provide a platform solution for a variety of architectures in the digital, mixed-signal, and RF domains.

The signal processing chiplets are assembled with RF circuits, fabricated with Infineon's mm-wave SiGe RF technology, and antennas included in the package. For this purpose, chip-first or RDL1st FOWLP technologies are investigated for their suitability for RF circuits and new process steps are developed.

Further development in the process blocks:

- Evaluation and characterization of new materials for release layers, spin-on dielectrics, and mold compounds.
- Systematic studies to increase wiring density through smaller track widths and spacing, reducing via diameters and increasing the number of wiring layers

FOWLP technology is suitable for combining heterogeneous chips as well as passive and other components in one package. This makes it possible to realize cost-effective systems-in-package (SIP).

The polymer rewiring of the electrical connections in the package between the chips minimizes parasitic effects. The packages are suitable for RF systems such as radar and 5G/6G modules.

This work is accompanied by electrical (RF) and thermomechanical simulations to create and validate the associated models and evaluate failure behavior under stress.

Radar applications:

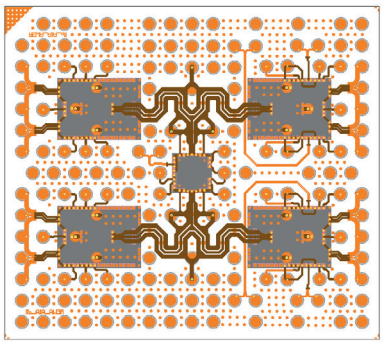
- Autonomous driving
- Harsh environmental conditions

Other applications for SIPs with chiplets:

- Automotive
- Service robots
- Smartphones
- Wearable devices

Project Status (10/2023):

- Construction of the technology demonstrator completed
- Production of the functional demonstrator in progress



RDL-1st-Design for REWAL

More information

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