Fraunhofer IZM

Fraunhofer Institute for Reliability and Microintegration IZM

Department

Wafer Level System Integration Berlin

Full-field projection laser scanner lithography (200–300 mm wafer size)

Semi-automatic electroplating tool with five different plating baths (100–300 mm wafer size)

Advanced microelectronic packaging technologies are tremendously important for successful implementation of todays and tomorrows electronics. With its application-driven research, Fraunhofer IZM bridges the gap between microelectronic component providers and technical system manufacturers in a broad range of industries, including automotive, medical and consumer electronics sectors. Since its establishment in 1993, Fraunhofer IZM has enjoyed a successful cooperation with TU Berlin's Research Center for Microperipheric Technologies with 450 highly trained employees.

The Wafer Level System Integration (WLSI) department is dedicated to the development and application of thin film processes for microelectronic packaging. ISO 9001:2015-qualified clean room facilities in Berlin and Dresden with production-compatible equipment enable cooperations with partners from the microelectronics industry and scientific community around the globe. The well-established wafer level pilot line can be utilized for prototyping and small volume production with technologies like wafer level bumping, wafer level CSP and redistribution, 2.5D/3D integration, flip-chip assembly, or MEMS integration. It also offers high flexibility regarding wafer sizes from 100 mm to 300 mm. Beyond silicon, wide bandgap and III–V semiconductors as well as glass, ceramic and molded wafers can be processed. For higher production volumes, the technology transfer to SME partners can be supported with our knowhow and experience from numerous R&D projects.

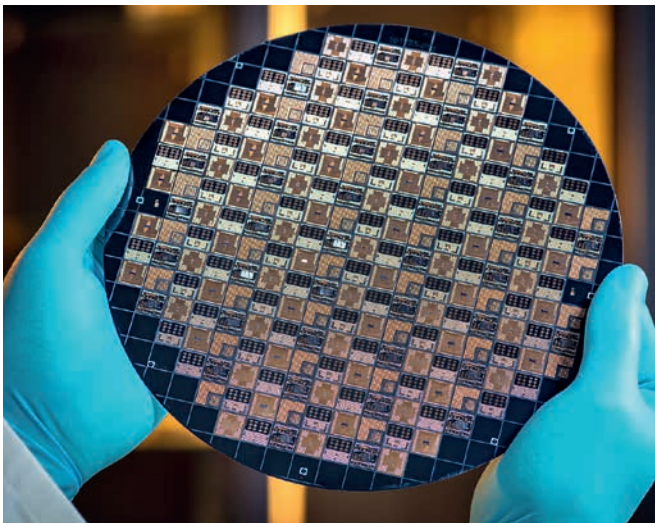
WLSI core competencies

- Wafer bumping: High aspect-ratio resist patterning for semi-additive structuring, copper pillars, high-density micro bumping, materials: Cu, Ni, Au, Sn, SnAg, AuSn, In, InSn, nanoporous Au (NPG)
- Assembly technologies: Die to die (D2D), die to wafer (D2W), wafer to wafer (W2W), die to board, module to board, reflow soldering, thermo-compression bonding, thermo-sonic bonding, diffusion bonding
- 2.5D and 3D integration: Through-silicon-vias (TSV) and through-glass-vias (TGV), thin wafer handling, wafer front-side and backside redistribution
- Thin film multilayer: Customer-specific layouts, multilayer routing based on Cu, Al or Au, integrated passives, RDL first or last, high-density flex
- Wafer level CSP/SiP: Cu redistribution, organic/inorganic dielectrics, package singulation, wafer and die thinning, fan-in and fan-out wafer level packaging, and reliability investigation
- MEMS packaging: Hermetic and quasi-hermetic capping of MEMS (fabrication of customer-specific cap wafers, wafer level capping by cap transfer bonding)
- Microsensor development: Design, development, and fabrication of various µ-sensors (also for harsh environments), sensor integration and packaging
- Photonic system integration: Design and characterization of photonic components or systems, optical co-designed packaging (CPO), integration of photonic components on interposers (e. g. reflow assisted self-alignment)

ISO 9001 2015 CERTIFIED

Fan-Out Wafer Level Packaging

Embedding singularized known good dies (KGD) in an epoxy molding compound (EMC) wafer and using WLP technologies opens up a broad field for innovative and cost-effective packages. Fraunhofer IZM has developed an RDL processing technology that uses EMC wafers with embedded silicon and/or III-V chips. This allows the individual wafer level packaging for single chip devices taken from a multi-project wafer. Small chips with a high-density I/O count can be embedded in EMC to generate larger fan-out routing. This allows their cost-effective matching to the large pitch of commonly used PCBs. By embedding multiple chips from different front-end technologies in one wafer together with wafer level routing, ultra-high density wafer level systems-in-package can be produced with low inductive connections. The interconnections between the chips are formed by thin-film redistribution layers, avoiding the need for the solder metallization of each chip of the final system.



Multi-project FOWLP wafer with RF chips

The EMC wafer has a lower temperature budget than the silicon wafer. Therefore, low temperature cure polymers based on PI, BCB, or PBO are used for multilayer RDL generation. The low-loss characteristics of EMC substrates in combination with the shortest possible interconnections length makes fan-out wafer level packaging attractive for highly efficient RF applications. RF test structures with low-k dielectrics have been constructed and proven to have excellent RF properties. Signal transmission of 90 % over a length of 6 mm has been achieved at a frequency of 40 GHz. Packages for applications with frequencies of up to 110 GHz have been also realized in fan-out wafer level packaging.

Cross-section of FOWLP of an RF chip in EMC with multilayer redistribution and solder bump

High Density Solder / Pillar Bumps and Metal Bump Interconnects for Fine Pitch Assembly

Solder bumps, pillar bumps and metal interconnects for flip-chip assembly are deposited by electroplating on the I/O pads of the chips with dimension below 5 µm diameter or up to 100 µm height. These chips can be flip-chip bonded by reflow soldering, transient liquid phase bonding (TLPB), thermo-compression and thermo-sonic bonding. High accuracy flip-chip bonders are used for flip-chip assembly with a position accuracy of 1 µm. The following materials are available for interconnects: Cu, Ni, Sn, SnAg, In, InSn, Cu pillars, AuSn, Au, Ag, nanoporous gold (NPG). In addition, advanced supporting processes, like reactive and inert gas ion milling of thin metal films or bump height levelling are available.

One key application for high density micro bumps at wafer level is the fabrication of hybrid pixel detector modules for imaging and particle tracking in high energy physics. These modules consist of one or more electronic readout chips, flip-chip bonded onto the sensor chip. In this case ECD bumping can be used for pitches even below 20 µm. Up to 6 million 30 µm pixel interconnection bumps are produced on 200 mm wafers with a 3-sigma uniformity of 2.7 µm.

Another key application are solid state pixel detectors. Especially for medical applications, x-ray detection cameras with high-Z detector materials, like CdTe or CdZnTe, come into focus due to their excellent absorption behavior at higher radiation energy. Sensors made of these materials are quite sensitive and require low bonding temperature and low bonding force.

Cryogenic electronic packaging is another emerging application field which requires soft and ductile solder materials like Indium to achieve a reliable interconnect even at very low temperatures below 10 K.

Single chip bumping

Due to high costs of full wafer tape outs in early R & D project phases, multi-project-wafers (MPW) are commonly used, delivering single dies. Fraunhofer IZM offers bumping services for single dies in order to support customers already in the early R & D project phases. The process was successfully demonstrated with Cu-pillar, Cu-SnAg solder and Ni-In solder bumps with a minimum pitch of 25 µm. Other ECD metals are possible as well, however, minimum structure size depends on the die layout. Up to several hundred chips can be processed on one carrier wafer.

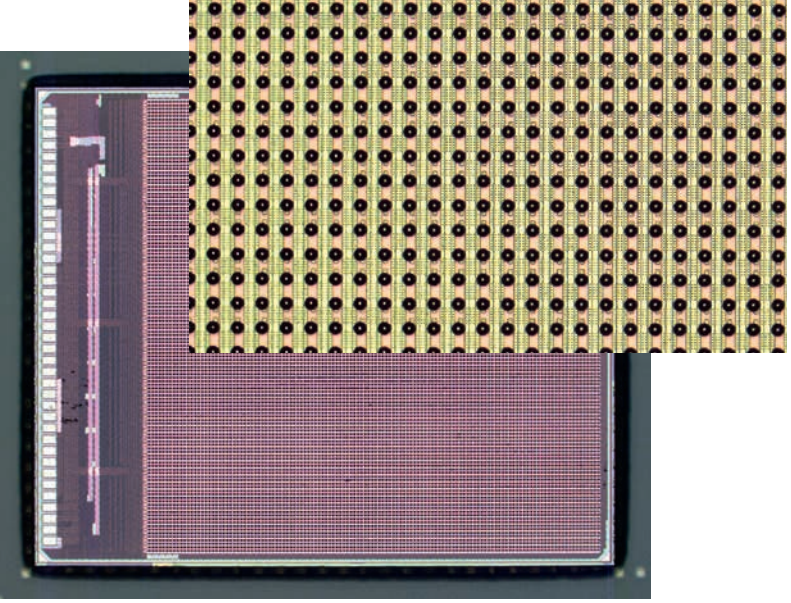
Single chip bumping can also be done by stud bumping, utilizing modified wire bonders and Au wires (Cu, Ag, Pt). The studs can be used for thermo-compression flip-chip bonding or adhesive joining with bond pad openings of at least 40 µm and a pad pitch at least 60 µm. The typical height after bonding is 20 µm.

Fine pitch assembly

For flip-chip assembly, bumped wafers from a fab supplier or in-house processed wafers are used. Assembly technologies involve semiconductors like Si, SiC, GaN, GaAs, InP, Ge and others, but also borosilicate glass, sapphire, quartz or fused silica come into play. Non-destructive and destructive testing methods are available, combined with cross-sectioning and advanced analytical tools, to qualify the results. For reliability assessment, we provide standard environmental tests (high temperature storage or temperature cycling) as well as specific methods as hermeticity or electromigration tests. Assembly methods are based on pick & place combined with subsequent reflow or thermode soldering, both usually fluxless. For thin chip assembly with > 20 µm thickness, we developed appropriate handling processes and tools for die picking from dicing tape and chip bonding to the substrates.

Low temperature bonding

Low temperature bonding is important for the assembly of components with different coefficients of thermal expansion (CTE) or temperature sensitive materials. With Indium bumps,



Single chip bumping: Individual die on carrier wafer after Cu-SnAg bumping, bumping pitch 25 µm

temperatures below 200 °C can be used for flip-chip soldering. Nanoporous gold (NPG) is used for thermo-compression bonding down to 150 °C. With thermo-compression bonding of Indium bumps to Au finish, we can reduce bonding temperature to 80 °C, with In-In even to 30 °C close to room temperature.

Nanoporous gold (NPG)

NPG has an open porous microstructure and is highly compressible which allows accommodation to topography (e. g. passivation steps). Microbumps below 5 µm pitch were demonstrated. The high compressibility and the large surface area reduces bonding pressure and bonding temperature drastically in comparison to bulk gold bumps. Flip-chip bonding on flex and on standard PCB materials is possible. In addition, the NPG can be combined with a pre-applied underfill material.

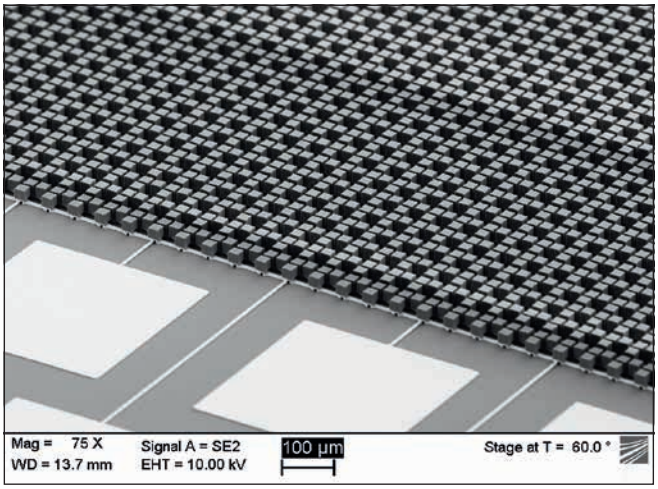
High precision bonding

Optical coupling between photonic integrated circuits (PIC) and III-V components like laser diodes and photodetectors require precise positioning of tiny optical facets. We apply assembly methods for edge- and grating-coupling schemes, using passive alignment methods which are supported by mechanical stops in silicon cavities processed on PICs or silicon optical benches.

High precision flip-chip bonding with sub-micron accuracy is one approach to precisely align and bond components, e.g. using gold bumps or nanoporous gold (NPG) in thermo-compression bonding. Position accuracy is achieved using machine vision, fiducial recognition, automated alignment and bonding. In a second approach, solder-assisted self-alignment during reflow soldering is applied, whereas intentionally misplaced components are pulled into place during the reflow process due to liquid surface tension and assisted by mechanical stoppers.

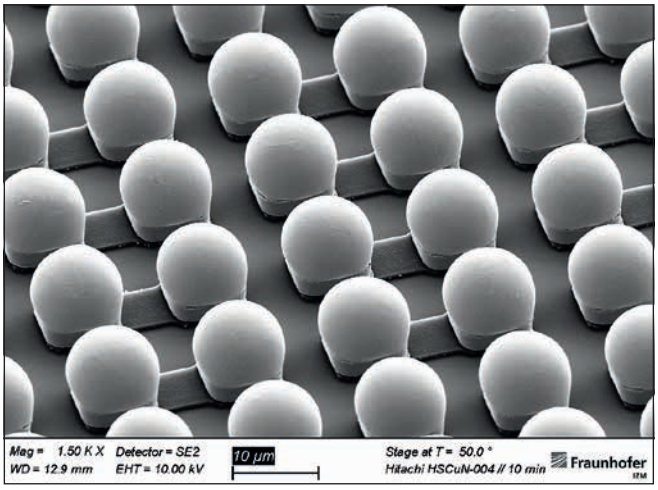
Micro-transfer bonding: Massive parallel assembly

This process allows massive parallel assembly of small chips which are too small for single handling. A vast number of chips is picked in parallel, transferred to the target substrate and finally the chips are soldered. We use a temporary bonding and laser release technique and demonstrated the assembly with 17,000 devices with components in three steps using AuSn for flip-chip attach. The method does not need any pre-treatment on the supplying die wafer like tethering and is compatible with flip-chip and high temperature bonding.



Micro-transfer bonding of 17,000 chips of 22 x 22 µm² size onto redistribution chip

SEM view of In-bumps with 15 µm pitch

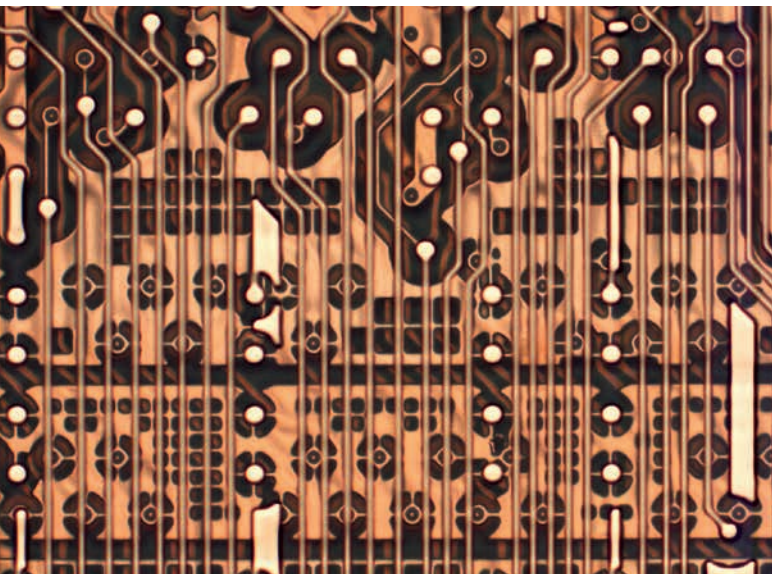


Key Technologies for 2.5D / 3D Integration

Thin film polymers

Polymers are the key building blocks for WLP and related technologies, including redistribution layers, integrated passive devices (IPD), and 3D systems-in-package (SiP). Several types of non-photosensitive and photosensitive polymers are available at Fraunhofer IZM, such as Polyimide (PI), Benzocyclobutene (BCB), and Polybenzoxazole (PBO). The choice of the most suitable material depends on the requirements of the target application, such as the operating conditions and reliability targets.

Test structures are available for a wide range of mechanical and electrical property characterizations to generate the data for optimized processes or process simulations. The thermo-mechanical properties exert a lot of influence on the reliability of non-underfilled WLP. Following trends in ultra-thin packages, thermo-mechanical stresses in polymers affected by cure temperatures can be analyzed in combination with CTE, water uptake, aging effects, fracture toughness, or adhesion to prepare for a multilayer package with excellent reliability.



4-Layer redistribution with Cu-wiring and PI dielectric

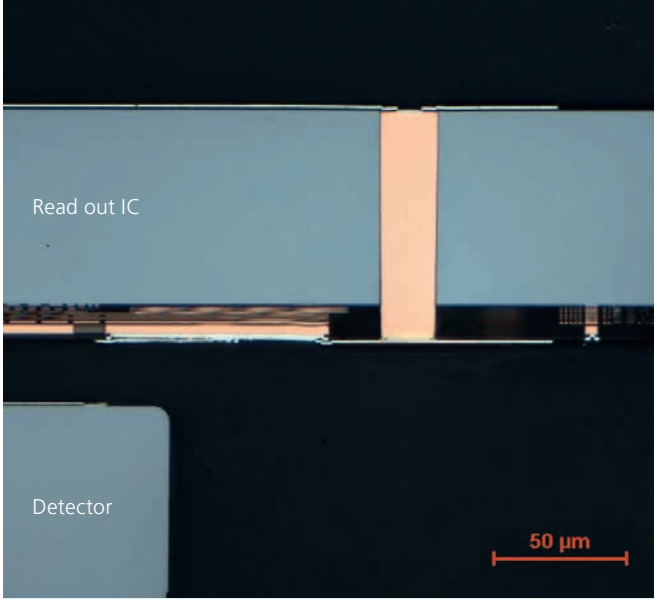
Redistribution layer (RDL)

Redistribution refers to the process of creating an interconnect structure on the top surface of a semiconductor device that redistributes its peripheral electrical I/Os to an area array arrangement. The RDL typically consists of one or more metal tracks (copper, gold or aluminum) and organic or inorganic dielectric layers to connect the bond pads on the active device to the new created flip-chip interconnects. This technology allows a high degree of miniaturization and integration, as it eliminates the need for wire bonding. Wafer level RDL is commonly used in mobile and consumer electronics, automotive, and medical applications, and its popularity can be expected to grow due to its benefits in terms of cost, performance, and reliability. Single or multi-layer redistribution is achieved in a semi-additive process for copper routing down to 2 µm on different substrates, including (ultra thin) silicon, glass, III–V semiconductor, SiC, or epoxy mold compounds (EMC).

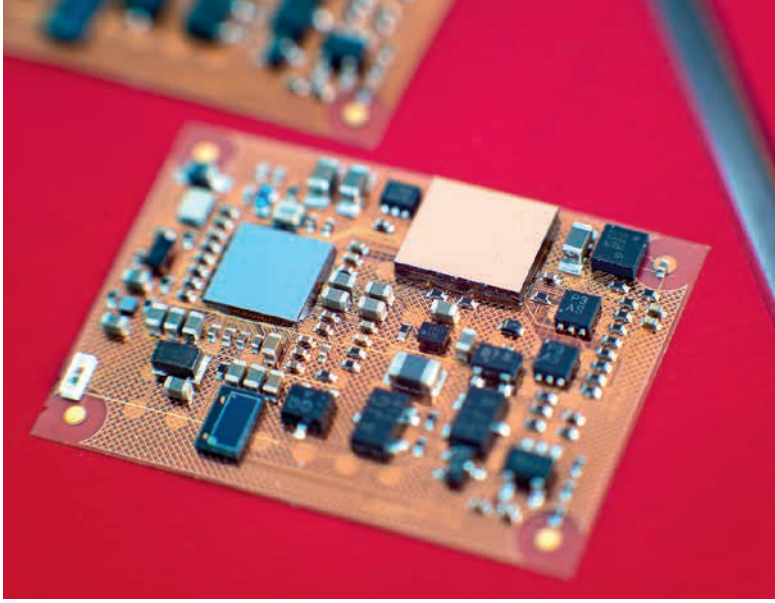
Design variants can be realized on wafer level by using a mask aligner with full-field exposure masks or laser direct exposure (355 nm). The RDL technology is used to produce CSPs with fan-in and fan-out routing, substrates with high density routing as well as TSV or polymeric interposers.

2.5D / 3D integration using TSVs in CMOS, silicon, or glass wafers

Through-silicon-vias (TSV) and through-glass-vias (TGV) are used for the heterogeneous 2.5D / 3D integration of multiple devices such as sensors, ASICs, processors, memory units, and transceivers with excellent electrical performance in a small form factor to support customized 3D systems. The TSV / TGV technology is combined with multilayer RDL technologies based on electroplated or sputtered metal tracks with organic or inorganic dielectric layers for insulation. High-performance signal transmission can be achieved by copper routing and low-loss polymer dielectrics for the RDL.



Read out IC (ROIC) with front side TSV last assembled on detector die



Assembled polymeric interposer based on thin film flex technology

The basic technologies for fabricating TSVs in CMOS or bare silicon wafers are dry etching of vias into BEOL and bulk silicon, CVD of insulation layers, and filling of the vias with electroplated copper. Multilayer routing as well as wafer thinning and thin wafer backside processing enabled by temporary wafer bonding are included in regular process flows.

TSVs can be formed from the front and the back side of CMOS wafers. In the latter case, the TSVs connect to metal pads which are present in the bottom layers of the ICs' front metallization layers (BEOL). This approach is particularly interesting for sensor packaging, as their sensing area can be maximized by routing all I/O signals directly to the backside of the devices to support integration via flip-chip bonding.

New cost-effective technologies for TGV formation have made glass attractive as a substrate for the 2.5D/3D integration of RF modules and sensor packaging with high wiring density as well. Fraunhofer IZM has developed a TGV metallization process that generates hermetically filled or liner-coated vias in a low-cost process without CMP and grinding required.

Polymeric interposers based on thin film flex technology

Already known in wafer level RDL, polymer-based multilayer I/O routings can be processed as fan-in or fan-out redistribution on the surface of ICs to reorganize their contact grid. A similar technology can be used to create ultra-thin polymeric interposers on which ICs or other components are mounted. The so-called thin film flex technology offers the same routing density as on chip wafer level redistribution and, at the same time, much greater potential and flexibility for high-density routing than standard thin coreless organic interposers.

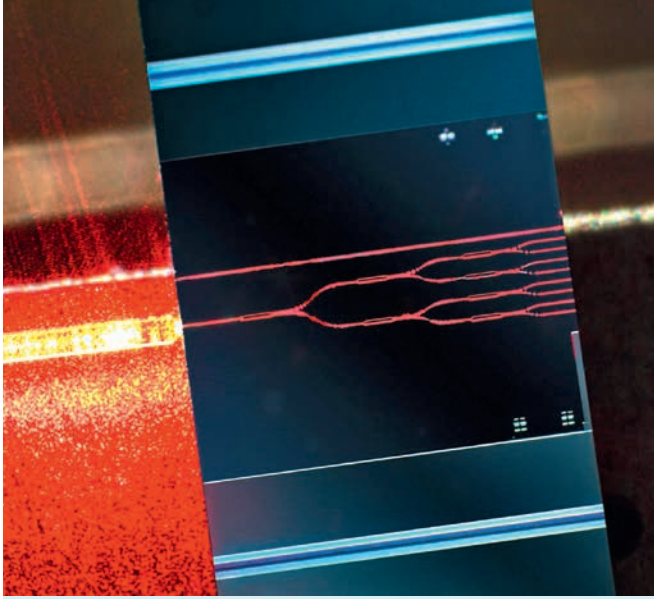
These polymeric interposers are fabricated with multiple copper routing layers and related inter-layer polyimide dielectric on temporary carrier wafers by repeat metal and polymer deposition and structuring. Depending on the required thickness of the metallization layers, typically in the range of 2 to 5 µm, fine line pitches of currently down to 8 µm can be enabled. The thickness of a single inter-dielectric layer is typically in the range of 5 to 10 µm. As pad finishes, metallizations like Cu, Au, NiAu or solders are available to enable different assembly processes.

As an additional feature, the technology allows the embedding of thin ICs or sensor components into the interposer RDL. To enable that, thin devices with maximum thickness of 20 µm are die-bonded at dedicated positions on the surface of an inner polymer layer. A following overcoating with polymer covers the thin devices completely. To access their I/Os, vias are opened through the top polymer layer and electrical connections are then established by the following wiring layer.

The resulting multilayer build-up is finally detached from the rigid carrier wafer using a high-speed de-bonding process. As a special feature, the technology allows the partial release of the carrier substrate in dedicated areas to create rigid and flexible zones in a single circuit.

Silicon interposer with two accelerator compute units and two high bandwidth memory (HBM) stacks for high performance computing (Chip/system design: ETH Zurich, interposer finish and chip assembly: Fraunhofer IZM)

Photonic System Integration



Light coupling from glass fiber to photonic integrated circuit (PIC)

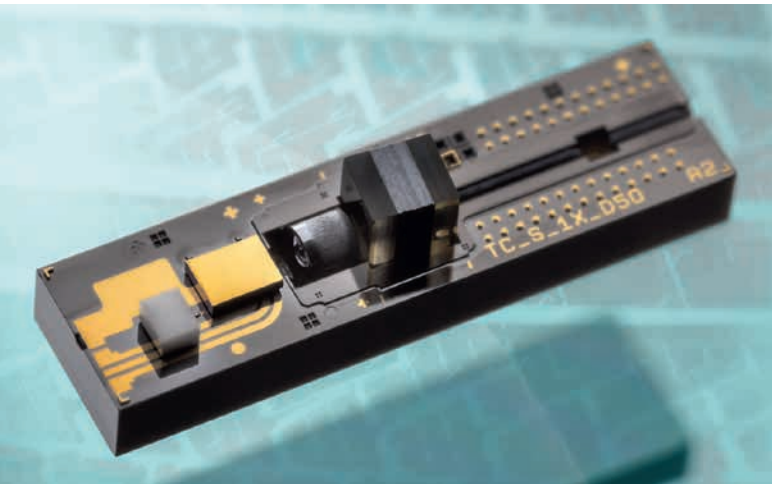
Looking for cutting-edge solutions in communication engineering, neuromorphic computing, and sensing technologies? Look no further than our leading group of engineers and scientists. Our expertise lies in designing and developing photonic microelectronic components and circuits. A wide range of services to help you achieve your goals can be offered.

The team is specialized in optimizing and tailoring solutions to the customers' requirements, taking into consideration factors such as performance, reliability, and manufacturability to ensure top-quality results. The portfolio includes project management and coordination to ensure seamless collaboration between the partners along the entire value chain, optimized resource allocation, and the holistic orchestration of workflows.

The customized photonic integrated circuits are designed and optimized using different material platforms, such as Si, III-V, polymers, dielectrics, and plasmonics, to ensure efficient cost and performance. Optical system integration solutions are provided, based on our extensive multi-disciplinary experience with wafer level assembly and packaging to provide the highest density of electrical and optical interconnects.

Characterization and benchmarking services for chip, wafer, and system-level RF investigations up to 500 GHz can be carried out, as well as performance testing for PAM4/16 256QAM modulations for next generation high-speed interconnects using 35 GHz AWG and 70 GHz RTS. Statistical and AI-assisted data post-processing is applied to extract valuable insights from complex datasets. By combining algorithms with advanced statistical techniques, we are able to analyze large data volumes in real time, enabling more informed decisions and uncover hidden patterns and trends that might otherwise go unnoticed.

The goal is to demonstrate groundbreaking achievements in the rapidly evolving fields of communication, computing, and sensing by creating next-generation systems that are faster, more efficient, and more effective.

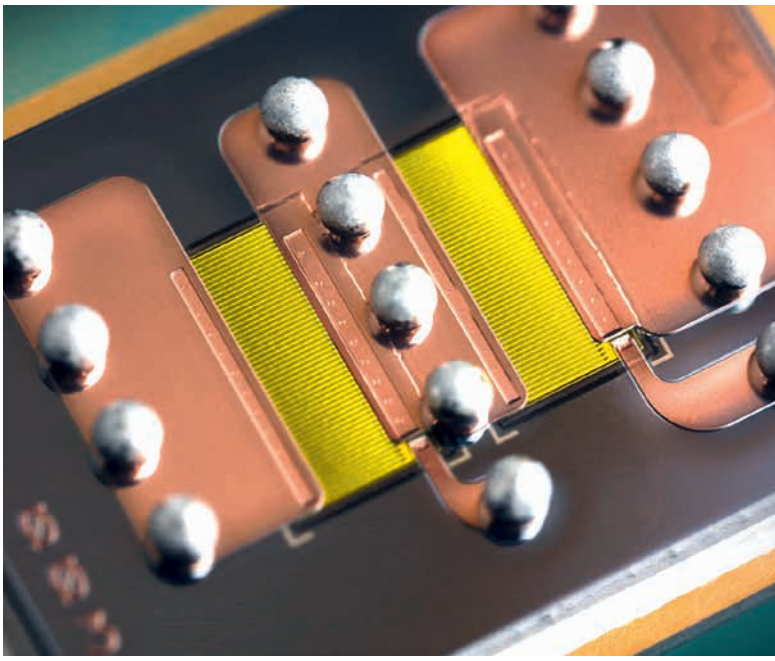


100 Gb/s data center transmitter module, flip-chip assembled athermal InP EML on silicon bench using solder assisted self-alignment scheme with 3D mechanical stops

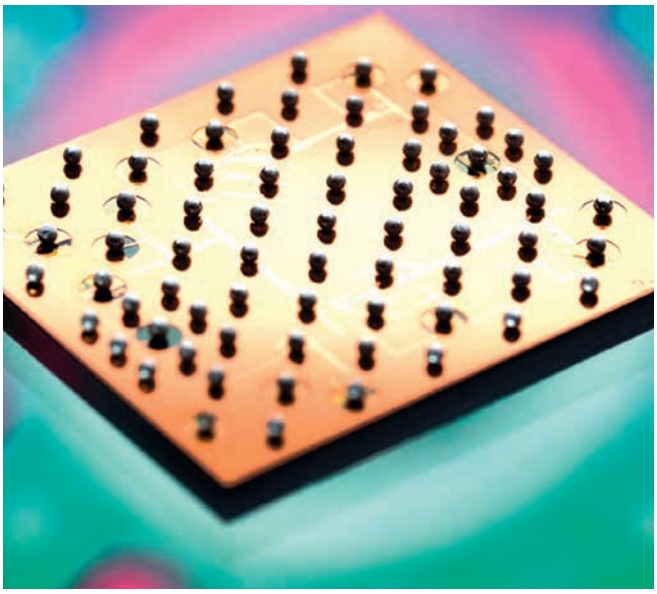
Power Electronics: Thick Cu Plating and Embedded Silicon Fan-Out Packaging

Wide bandgap semiconductor materials like GaN and SiC are getting increasing attention, as they allow higher switching frequencies and thus enable higher efficiency as well as lower loss, leading to increased power density and more compact modules. This requires further improvements in power management, high current feeding, and high voltage insulation. Suitable metal finishes like thick Cu or Ni-Au pads are offered for IGBT and diode wafers (100 mm, 150 mm, 200 mm) for chip embedding, silver sintering, transient liquid phase bonding (TLPB), or Cu bonding.

Solutions compatible with high temperatures are used, including TLPB using Cu/Sn, AuSn soldering, Au-Au and Cu-Cu thermode bonding, nanoporous gold (NPG), or sintering using silver die transfer films. New package solutions are developed based on double-sided cooling by preparing the wafer on its front and backside and by selecting materials with fitting thermal expansion and using joining methods capable of operating in high temperatures to achieve highly reliable modules for extreme thermal requirements. The 3D stacking of power devices further reduces the footprint of the modules.



Embedded GaN half bridges in silicon



Highly planar modules for stacking with thermal interlayers are formed by embedding power devices and drivers into thick silicon interposer substrates, resulting in an embedded silicon fan-out package (eSiFOP). Wafer level processing for cavity formation, die attach, dielectric insulation, and the electroplating of thick copper for power distribution is used to facilitate batch manufacturing at reasonable costs.

Thick Si, SiC, or diamond wafers ensure robustness. As a planar heat spreader, they are excellent interfaces for thermal management.

Multi die embedded silicon fan-out package (eSiFOP) with Si, GaN and SiC components

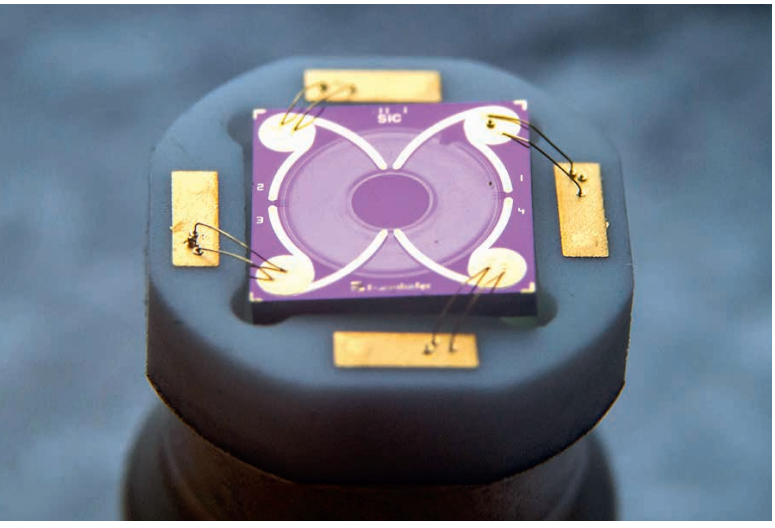
Microsensor Development and Integration

Microsensors are widely used in a range of applications including automotive, entertainment, industry, mobile, and IoT applications, especially due to their small form factor, light weight, and low production costs. Many years of experience in the field of semiconductor and sensor technology make us the ideal partner for your sensor needs.

We have the know-how and technology for device development, prototyping, testing, and low volume production of microsensors, with a complete R&D pilot line: Beginning with the requirements or concepts, the FEM-based sensor design and manufacturing of sensor elements on up to 200 mm wafers, and the support of packaging and testing for sensors that measure physical parameters, e. g. pressure, acceleration, or force. For the realization of micro-mechanical sensors, different physical effects can be used to achieve sufficiently high sensitivity and the required linearity.

Piezoresistive pressure sensor with 0.8 mm² footprint

Piezoresistive silicon carbide pressure sensor for applications above 400 °C



Services across the entire manufacturing process chain are offered, including wafer level bonding by anodic, direct, or fusion bonding and thin glass layer bonding, as well as standard and customer-specific packaging with integrated data processing, e. g. TO8 packages with media separation and molding.

Different metallization systems can be applied to the sensors to prepare them for moderate or high temperature applications.

Pressure sensors

- Miniaturized pressure sensors (1–400 bar, up to 125 °C)
- High-pressure sensors (up to 1000 bar, up to 125 °C)
- Low pressure sensors (< 100 mbar with a sensitivity range of several µV/VkPa, up to 125 °C)

Gas sensors

- Hydrogen gas sensors working at room temperature

Sensors for harsh environments

- SOI-based mechanical sensors for temperatures up to 400 °C
- SiC-based sensors for temperatures above 400 °C

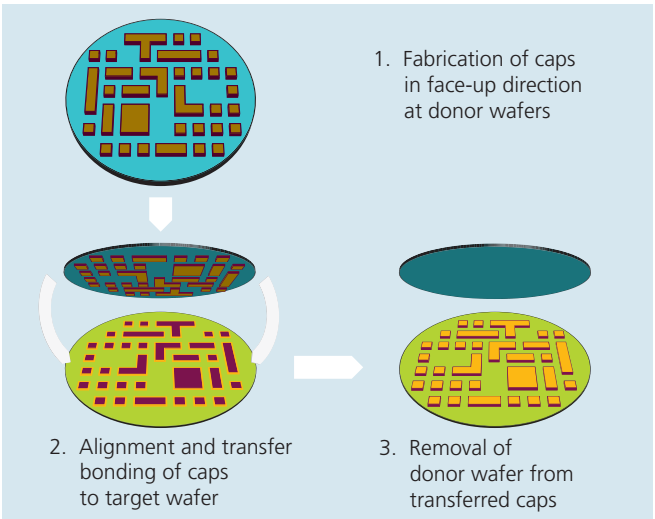
Wafer to Wafer Bonding, Capping and Hermetic Sealing

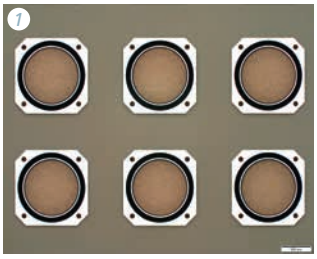
A broad range of permanent and temporary wafer to wafer bonding technologies are available, enabled by semi or fully automated alignment and bonding equipment. The processes are based on anodic bonding, direct or fusion bonding, thermo-compression bonding, transient liquid phase bonding, soldering as well as low temperature or even room temperature adhesive bonding. Metallic bonding materials such as AuSn, CuSn, Au-Au, Cu-Cu are deposited by semi-additive, subtractive, or lift-off processing. The adhesives for permanent bonding, including thermally or UV curable polymeric materials, are deposited by spin/spray coating or lamination techniques and structured by photopatterning, transfer printing, dry etching or laser ablation. Temporary bonding for handling wafers with thicknesses down to 30 µm is enabled by non-permanent adhesives and carrier wafers which are eventually removed by laser assisted or thermal slide-off de-bonding.

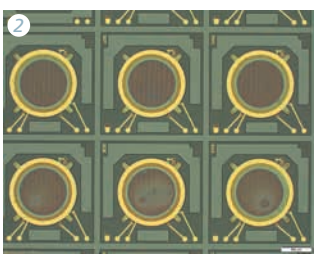
The typical applications of the available bonding techniques include thin wafer handling, hermetic, or quasi-hermetic bonding of recessed wafers for device protection and sealing, as well as functional stacking of active or passive devices like ICs, MEMS, spacers, or lens structures.

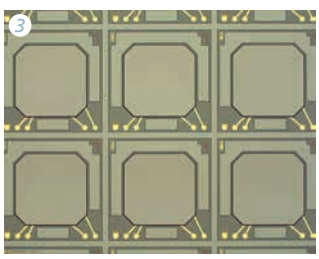
Hermetic sealing by bonding a cap wafer to a TSV device wafer

The large choice of permanent bonding options in combination with high-performance temporary bonding also allows the use of advanced technologies like wafer level device capping. Such approaches allow the placement or pre-processing of components or custom specific cap/lid structures on temporary carrier wafers. These so-called donor wafers are then used for the simultaneous transfer bonding of all components to a device wafer. This approach means that the transferred components can be laterally smaller than the landing devices on the target wafer, so that the peripheral I/Os on the landing devices are still accessible.









Left side: principle of wafer level capping

Images: (1) caps on donor wafer, (2) device wafer without and (3) with transferred caps

Cover:
Glass Interposer with
TGVs and assembled test chiplets

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