Smart PCBs Manufacturing Technologies

T. Löher[1], A. Neumann[1], L. Böttcher[2], B. Pahl[1], A. Ostmann[2], R. Aschenbrenner[2] and H. Reichl[1]
[1] Technische Universität Berlin, TIB 4/2-1, Gustav-Meyer-Allee 25, 13355 Berlin, Germany
[2] Fraunhofer Institut für Zuverlässigkeit und Mikrointegration, Gustav-Meyer-Allee 25 13355 Berlin, Germany
loeher@izm.fhg.de, phone.:++49-30-46 403-648, fax.: ++49-30-314-72 835

Abstract

The inherent functionality of a printed wiring board can be dramatically increased by embedding electronic components into the board. For resistors, capacitors and inductors technological turnkey solutions are offered by major manufacturers and also novel technologies are under development. Application examples for passives integration into flexible PCBs will be given. A further boost of functionality will be accomplished by the integration of active chips into the board. An overview of different approaches and the respective sets of enabling technologies for the integration of chips into the board will be given. Two of the approaches for the chip integration into the board will be discussed in detail. A prerequisite for those technologies is the chip thinning, which is now available as a commercial service for chip thicknesses down to 20 µm. In the chip in polymer (CIP) approach the thin chip is precisely positioned and soundly attached onto the board surface. After lamination of a copper coated resin foil via contacts are drilled through the laminate to the contact pads of the chip. The transfer of precise chip position parameters with respect to the board is essential for this step. The wiring on the laminate foil to the chip and to other components is subsequently structured. Process parameters and results will be presented. For the embedding of chips into flexible PCBs the chip is flipped onto the substrate surface and thermode bonded. The process implies soldering. Therefore electroless Ni(P) is deposited onto the Al bond pads of the chip which is subsequently covered with small caps of solder. The solder cap heights are in the range of 4 to 8 µm in order to keep the interconnection height low. The solder joint is realized by thermode bonding of the chip onto the structured wiring of the substrate using no-flow underfiller. The chip containing layer is then laminated and contacted to outer layers of the board by conventional through hole technique. An assessment of the advantages and disadvantages of both approaches will be given on the status of our present understanding of the technological challenges.

Introduction

Miniaturization and functional diversification are the most powerful development drivers in electronic industry. On the one hand the roadmap appears predetermined by Moores law, referring to semiconductor processing which then again affects electronic appliances in general. On the other hand diversification manifests itself by the progress and increasing importance of electronics in many application fields where hitherto electronics was not major function, e.g. the increase of electronic instrumentation and control in automotives, increasing functionality of mobile communication, and human body adapted medical applications. In different fields the requirements are very specific and generally differ considerably among each other. Specialized measuring, controlling or actuating functions are performed by dedicated electronic subunits, which generally require an electronic periphery that itself can reach a high level of complexity. At large, electronic systems are composed of parts which are fabricated with accordingly different and specific technologies, which have to be assembled using suitable electrical interconnections to provide electrical system integrity.

The common platforms for electronic assembly are printed circuit boards, either rigid or flexible polymer based materials or ceramics with metal wirings in one or multiple layers. Components and subsystems to be assembled are commonly arranged on the board surface. Corresponding to the electronic system, the routing of the metal wires within the board has a more or less complex 3 dimensional architecture. For almost four decades efforts have been made to reduce the component count on top of circuit boards, by embedding passive components into the circuit board. The obvious benefits to name only a few are (1) simplified and shortened wiring, (2) increase reliability by reduction of solder joints, and (3) better electrical performance by reduction of parasitic effects [1]. A multitude of technologies for the embedding of passives into circuit boards is now available from different vendors. Some of these technologies will briefly be described in subsequent sections.

The performance density of electronic systems will experience a further dramatic increase by the embedding of active chips into the circuit board: thereby the board itself will become the package for more complex subsystems. The type of embedded chips can cover the whole range from

simple arrays of passives to integrated passive networks or active ICs [2 - 4]. I the following section a very brief overview of passive embedding will be given, stressing the recent approaches and limits of the commercially given technologies. The next section will describe three chip embedding technologies two of which will be addressed in more detail.

Passives Embedding Technologies

For the embedding of passive components different technologies and issues have to be mastered, since rather large ranges of values with tight tolerance for resistors, capacitors and inductors are required for given applications. It should be mentioned that in most of today electronics applications the ratio of capacitors to resistors to inductors is far more than 50% to less than 40% to less than 10%. Components and some commercially available technologies are the following:

Embedded capacitors:

The process technology for embedding of capacitors is for most of the commercially available products more or less the same: 1. capacitor sheets are purchased from the supplier, 2. the sheets are structured on one side, then laminated onto the substrate and subsequently structured on the other side to form the counter electrode. Although the process technology is similar, due to the different materials and technologies to apply the dielectric, sheet capacitances cover a wide range. Dielectrics are classified into paraelectrics (low ε_r) and ferroelectrics (high ε_r). The former generally result in low sheet capacitance values, but the electrical performance of paraelectrics is better due to higher stability under temperature changes and less sensitivity to frequency and bias voltage (generally decreasing with applied frequencies and voltages). The use of embedded capacitors especially for the power distribution system in the periphery of an active device offers many advantages over the conventional surface mount devices [1].

Embedded resistors:

(i) Stencil or screen printing of resistive pastes (generally carbon particle filled polymers). Large resistor value ranges can be covered with appropriately adapted paste compositions. Tolerances of the as printed resistors, however, are much too large for most applications. Therefore generally printing has to be followed by laser trimming of the resistors. The effect of subsequent lamination into an inner layer of the board is yet another issue impeding the easy use of this technology.

(ii) Thin film technologies are available that allow resistors to be fabricated with a smaller value spread even without additional trimming, e.g. ± 4% [5]. Application of the resistor structures onto the board can be achieved by lamination of copper sheets that are coated with a thin film resistor layer (Ni or Pt resistor layers [6,7]) followed by a two step structuring/etching processes, or additive plating (electroless Ni(P)) on prestructured substrates. A drawback with this technologies is that sheet resistances are today limited values between 250 (Ni) and 1000 (Pt) Ohm/square. Thus reasonable resistor values are limited to values below 10 kOhm. Yet another problem is that power dissipation capabilities generally decrease with increasing sheet resistance.

Embedded inductors

For the embedding of inductors no additional technology is necessary. Spiral or rectangular inductors can be patterned directly on a metal layer on the circuit board. However the electrical properties have to be simulated and tested in detail for any give combination of metal wire geometries and embedding materials.

Embedding of Active Devices

Three alternative technologies for chip embedding will be presented in the following. All of the presented technologies emphasize exploit as far as possible base technologies that are today in use at common printed circuit board manufacturers.

Integrated Module Board Technology

In the late 90s at Helsinki University the integrated module board (IMB) technology was developed [10]. Starting with a conventional rigid substrate core material after structuring of the metal layers a cavity with the lateral dimensions close to that of the chip is made through the core to take in the chip. A laminate layer to take up the chip is then applied to the board, whereon the chip is aligned and placed in the cavity using a high accuracy flip chip bonder. The alignment inside the core is better than +/- 5 µm. The cavities are then filled with a molding polymer that is chemically, mechanically and electrically compatible with the chip, the substrate and the build up materials. After curing of the thermosetting epoxy the laminate is removed and the board is cleaned from residues and impurities. The chip is now at the same level as the surface of the substrate. In the next step the core is laminated on both sides with a resin coated copper (RCC) foil. Microvias to the chips are fabricated using an UV-laser and metallized in horizontal plane plating line. The outer layers are manufactured by semi additive pattern plating and an alkaline etching process. Finally a solder mask is applied and the pads for the components are coated with an organic surface protection or a thin gold layer.

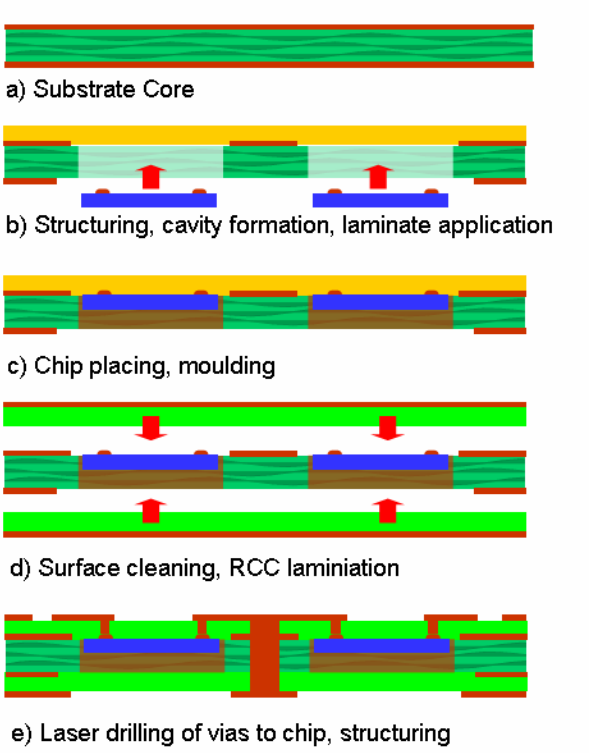

Fig. 1: Integrated Module Board technology process flow.

With the IMB technology it is possibility to embed components with a range of thicknesses; the only constraint is that the component thickness should not exceed that of the core layer. Generally wire board manufacturers are, however, reluctant to have a cavity in the core layer of the board. Undesired fragility can be induced into the board even after filling of the cavity with the molding material. The fabrication of the cavity depending on the applied method (punch through, mechanical drilling, laser drilling) is a cost factor.

Chip In Polymer

The technology developed at TU Berlin works without a cavity layer in the wire board. Here very thin chips are directly placed on top of the core substrate. Chips thinned down to 50 µm are placed and attached onto the board with high precision using adhesive or die attach film. Then the chip is embedded in a polymer layer by vacuum lamination. Vias to the chip contact pads and to the Cu-routing on the board are laser drilled and metallized. Finally the top Cu-layer is structured.

The structure now allows to position conventional components directly over the embedded chip.

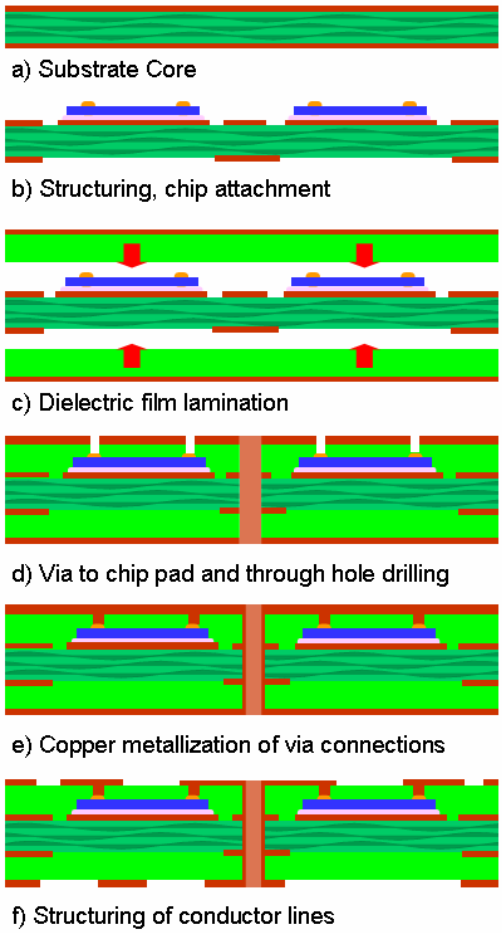

Fig. 2: Chip in Polymer schematic process flow.

In the following process details of the CIP process are described in more detail [11]. The process technology is at the moment under development for large scale production capabilities and supported by the European Union in the project HIDING DIES [12].

Wafer and chip preparation

Conditioning of the chips for the embedding process is most cost efficiently done in wafer level processes. First ((is not compatible with thin film)) the Al or Cu contact pads of semiconductor chips have to be reinforced in order to be compatible with the laser drilling of microvias and the PWB metallization process. For this purpose a 0.2 µm TiW/Cu film is sputtered / structured (Fig. 3) and finally reinforced by electro less deposition of 5 µm Cu. Thinning of the wafers to 50 µm is mainly performed by a subcontractor.

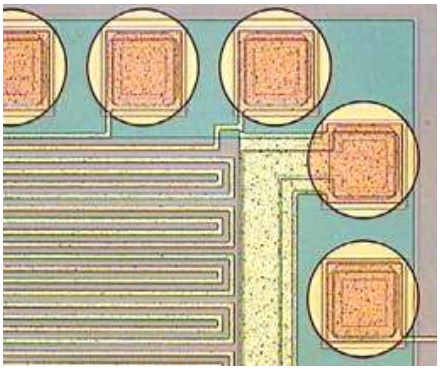

Fig. 3: Sputtered TiW/Cu layer over Al bondpads.

In the present technology development it is aimed to handle contact pitches of 150 µm by forming vias directly to the chip pads. Smaller pitches currently require a redistribution layer (RDL), which converts the narrow pitch of peripheral pads to a more relaxed area array configuration. In order to investigate the feasibility of this approach, a polyimide-based RDL was prepared on test wafers by a subcontractor (Flip Chip International).

For dicing, wafers are mounted to an UV dicing tape. A careful selection of dicing blades and parameters is necessary. After dicing, the tape is exposed to UV light. As an example the Lintec D-175 tape was exposed for 25 s @ 115 mW/cm² resulting in a very good picking performance with low remaining tackiness.

The die bond process

The challenge of thin die bonding is to achieve a low bondline thickness. The embedding into a build-up layer limits the allowed thickness of chip and die bond adhesive. Together it should be less than the dielectric thickness, leaving about 15-20 µm of dielectric over the chip after embedding. Otherwise a planar embedding is impossible and the chip might be damaged.

Screen printing allows a precise control of volume and location of the adhesive paste, which is more difficult to manage by dispensing. By using an electrically conductive Ag-filled paste a bondline thickness of 16 µm was achieved; see fig. 4.

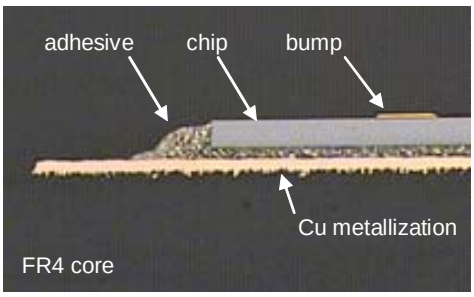

Fig. 4: 50 µm chip, die bonded using a Ag-filled conductive adhesive.

An alternative is the use of b-stage paste. After printing it is dried and becomes non-tacky. It allows a decoupling of printing and die attach. After drying boards can be stored or moved to other locations. During die bonding the boards or chips have to be heated in order to achieve again a surface tackiness. Chips bonded with b-stage adhesive have shown less voids compared to standard material.

Die attach film can also be used for the same purpose. It is a UV dicing tape which has two layers: a conventional UV dicing foil and an adhesive layer on top. Wafers are mounted to this adhesive layer. The dicing blade has to cut the silicon and the top layer of the tape. In the picking process this layer remains at the chip and serves as adhesive. In order to tack the chips to the substrate, it has to be heated.

The chip embedding technology needs a fast and accurate die bonder which is capable to handle 50 µm thin dies and which provides adjustable temperature for the bond head and the substrate chuck. This is provided by Datacon's 2200 apm+ platform.

Another challenge is to reach the required placement accuracy for the thin dies bonded on PCB layers. Since the copper structures of the layers are very sensitive to changes in illumination, the optical recognition on these substrates did not work properly when using the standard lighting. To overcome this drawback a new lighting system was designed which illuminates the substrate from a more obtuse angle.

For chip embedding accuracy plays a crucial role. The tolerances of the sequence die bonding, via drilling and Cu structuring have to be very low in order to achieve an acceptable yield. One requirement is that the machines for these three process steps use the same fiducials on the core for alignment.

Chip lamination

The chips are effectively embedded into the PCB structure by vacuum lamination. The core substrate with the die bonded chips is covered from both sides with a RCC layer. A press book consisting of separation films, pressure distribution material and steel plates is used. The vacuum in the press chamber ensures a void-free distribution of the RCC dielectric.

The lamination profile is a compromise between low pressure to protect the chips and high pressure for flow and curing. A high flow, high T_g RCC is used to obtain optimal results. The kiss pressure needs to remain low to prevent from introducing cracks in the silicon; however, a minimum level is required to sustain sufficient flow around the chips. The used RCC requires 40 min curing at a temperature above 175 °C. To minimize warpage, the boards are cooled under pressure at the end of the cycle.

As the HIDING DIES concept brings together materials with very different properties (especially CTE), warpage of the board is a concern. A symmetric build-up is a first requirement to avoid excess warpage. Core thickness is also an important warpage determining factor, as is indicated by the use of two different stacks: one with 0.6 mm core, one with 0.1 mm core.

An important parameter is the resulting epoxy thickness on top of the embedded die, after lamination. This thickness will determine the possibility for making small microvias for contacting the I/O pads of the chip. The uniformity of the covering epoxy layer is important for the process window of the laser drilling. Different factors as die bond layer thickness, thinned silicon die thickness and planarity of the lamination press will influence the uniformity. Because the bare dies are embedded in the build-up layer, the lamination thickness will also depend on the number of embedded dies, or the total surface taken by silicon. A 15 – 20 µm epoxy layer on top of the embedded die, as shown in figure 5, is considered a good compromise between laser drilling margin and ability to create small microvias.

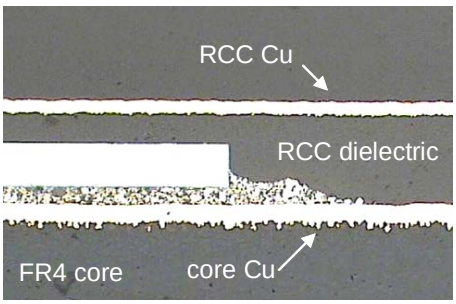

Fig. 5: Embedded chip in a RCC layer.

Via Drilling

The laser drilling of vias to the bond pads of embedded chips is comparable to the established formation of microvias on PCBs. Over the contact pads, holes are opened in the Cu layer of the RCC. Then the dielectric is removed by a laser until the Cu bump is reached. Finally the walls of the vias are metallized, as described in the following section. The challenges are in tight positioning tolerances and small via sizes

For the drilling process at TU Berlin a pulsed 355 nm UV laser is used. It ablates Cu as well as the RCC dielectric. The challenge is to choose laser parameters (drilling time and beam energy) which remove the polymer completely without cutting through the Cu bump. This can be achieved by first using a higher energy for Cu structuring, followed by slower drilling for dielectric removal.

In a production environment a dual beam machine first the top Cu layer is opened by a 355 nm UV laser, cutting only slightly into the dielectric. Then a fast ablating CO_2 beam drills down to the bump, without etching the Cu. The equipment cost is relatively high but this method allows the fastest drilling with speeds up to 150 holes/s.

Accurate alignment of the microvia drilling with respect to the underlying Cu pattern is crucial for the yield of the interconnection. With the current I/O pad pitch (min. 150 µm) and the enlarged Cu pads on the chips, alignment based on fiducials on each 10x10 cm² (sub-)panel are sufficient. For smaller pitches it is expected that local fiducials, closer to each chip, will be necessary.

Cu interconnect

After laser drilling the microvias are cleaned in a desmear step (KMnO4 @ 65°C). This is followed by Pd activation and electroless Cu deposition. The Cu layer is 1 – 2 µm thick and acts as a seed layer for the subsequent galvanic plating. A minimum thickness of 10 µm Cu is required in the microvias (figure 6 a) Some experiments have been done with reverse pulse plating in order to fill the microvias completely with Cu (figure 6 b).

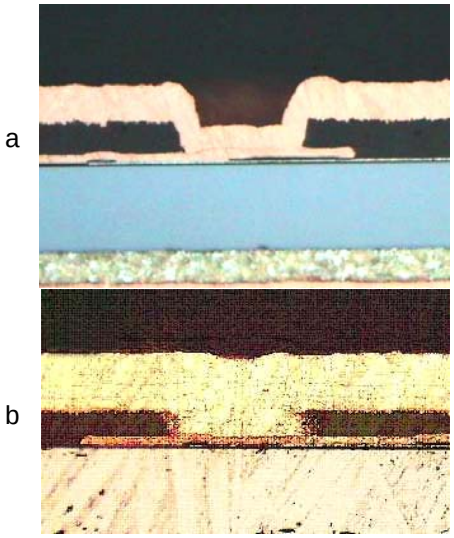

Fig. 6. Microvias to embedded chips metallized with electro less plating and (a) DC electroplating (b) reverse pulse plating.

The top interconnection pattern is realized by standard photolithography and acid spray etching (CuCl2:HCl). Again alignment of the pattern is a crucial step in order to achieve the fine pitch requirements of the embedded dies, see.

Daisy chain electrical measurements containing microvias to the chip and microvias to the core substrate have been done and show good uniformity of the contacts. Figure 7 shows a close view to one of the realized test vehicles. The good alignment between chip, via and metallization is clearly visible. A further example can be seen in figure 8. It is a cross-section of a module with 100 µm core. The total thickness of this very thin device is only 300 µm.

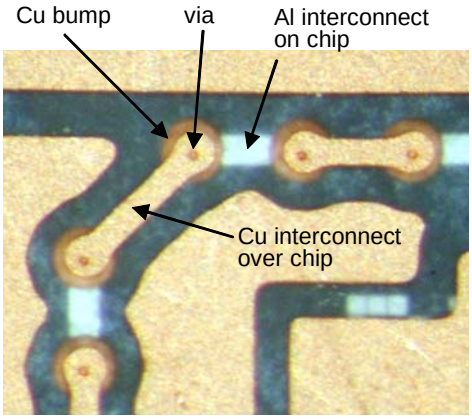

Fig. 7: Detail of interconnects from RCC layer to embedded chip pad.

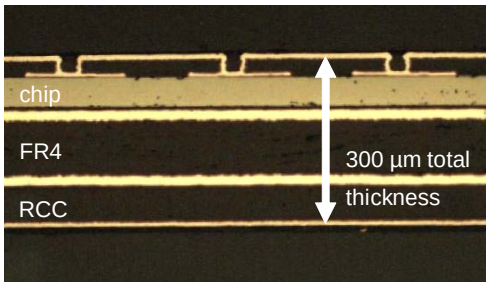

Fig. 8: Chip embedded in a substrate with thin core (via metallisation only by electroless Cu).

Chip Embedding into Flex

With the embedding of chips into flexible wiring boards the functional density of electronic systems can increased even more than with the above described technologies. The benefits of flex substrates, as light weight and high wiring density, will here be joined with the complexity of the active chip. However, in order to maintain the basic flex substrate characteristics, the build-up with an integrated chip has to be as small as possible. Chips with a thickness of only 20 µm are used and the interconnection should not exceed a couple of microns.

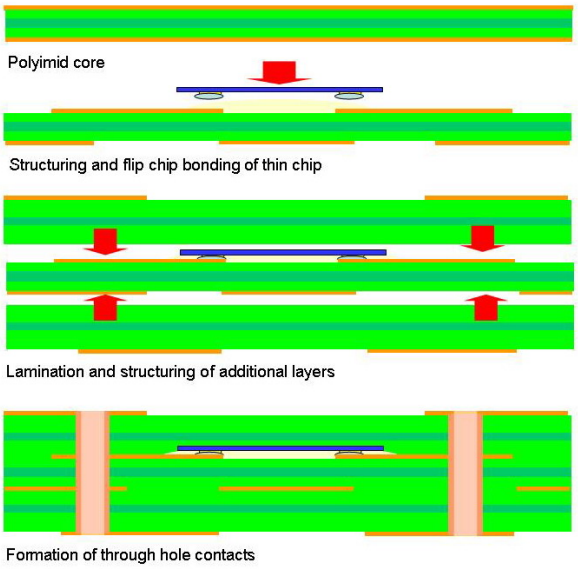

Fig. 9: Schematic process flow of embedding of thin chips into a flexible wiring board.

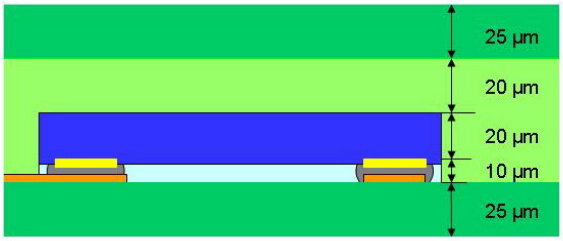

Fig. 10: Representation of a thin chip in the flexible wiring board.

The technology under development at TU Berlin is relies on a flip chip type mounting of the thin chip onto the flex substrate and laminate the structure on both sides. Contacts to outer layers are realized by through holes, see figure 9. Further layers can be processed on the build up. The electrical interconnections are extremely thin, as depicted in figure 10, and the mechanical coherence of the chip to the substrate is given by the no flow underfiller. Process technologies for embedding of passive and active components into flex wiring boards are developed and investigated in the European Union funded project SHIFT [12].

Wafer perparation

The electrical interconnection from the chip to the wiring of the flex substrate is an ultra thin solder contact. The solderable contacts on the chips are accomplished in a wafer level process before the wafer thinning procedure. First the bond pads of the chips are equipped with a solderable under bump metallization. Therefore Ni(P) is deposited in an electro less process onto the otherwise unsolderable Al pads of the chips. The Ni bump height is

within 3 and 5 µm (± 3 %). Onto the Ni bump SnCu solder is deposited by an immersion soldering process. The wafer is dipped into a liquid solder bath. Pulling the wafer out of the bath small solder caps are formed on the Ni. The average heights of the bumps depend on the size of the Ni pad (which is 40 µm for the test vehicle under investigation at TU Berlin); see figure 11. However, the variation in bump height for a given pad size is very large ± 50 % [12]. This variation is leveled out in the subsequent thermode bonding processes, where an excess of solder is squeezed to the side of the interconnection. At the interface between solder and Ni intermetallic phases form, still enough solder remains to allow for a subsequent bonding process.

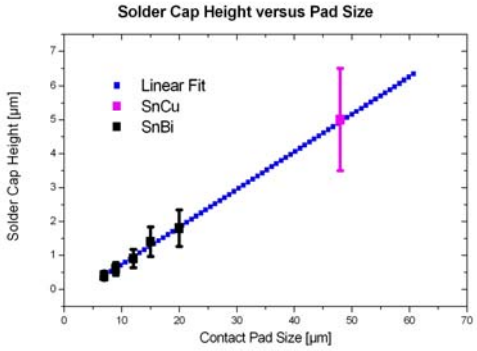

Fig. 11: Thickness of a solder cap after immersion into the liquid solder a function of the contact pad size.

Wafer thinning

The thinning process goes along with the dicing of the single chips. First the chips on the wafer separated either by sawing or by etching. The etching or sawing lines reach 25 to 30 µm deep into the wafer. In case of etching a conventional photolithography process is used. The advantage of etch separation is that mechanical defects at the chip edges are greatly reduced, as compared mechanical dicing. Edge defects are likely to be the starting point of chip fractured in subsequent processing steps.

After separation the wafer is attached to a UV-release grinding tape. The wafer is ground to a thickness of 50 to 60 µm in the first step at high speed (300 µm/min) then spin etched at a rate of 30 – 40 µm/min to the final thickness of 20 µm.

Proper release of the chips from the tape is crucial for the further processing. Especially the solder caps have to be free of any contamination in order to remain solderable to the flex substrate Cu wiring. UV release tape turned out to be best suited in with this respect.

Thermode bonding to the flex substrate

Single chips are subsequently thermode bonded to the Cu-wiring of the flex substrate. The flex polyimid (PI) is fabricated in a common way, using photolithography and etching of the Cu coating on the PI substrate. In order to keep the standoff between the chip and the substrate small, the Cu wiring height was prior to structuring etched down to a height of 7 – 10 µm, see figure 12.

Thermode bonding is performed with commercial flip chip assembly equipment. The use of no flow underfiller is crucial to warrant the integrity chip interconnection to the substrate and to make sure, that no voids or air bubbles remain under the chip after the subsequent lamination. The challenge turns out to be the dispensing of a suitable volume of underfiller. A too large amount results in an undesired flow of underfiller to the top side of the chip, too small an amount lacks to fill the gap between chip and substrate. With screen printing this problem could be well mastered. The underfiller height after printing is quite homogeneously 12 – 14 µm ± 10 % and the lateral extension of the printed patch has to be adapted according to the substrate Cu-line height such that underfiller is just squeezed to the edge of the chip.

Pressure and temperature profile of the bonder are adapted to the melting temperature of the solder bumps ~230 °C, and the curing characteristic of the no flow underfiller.

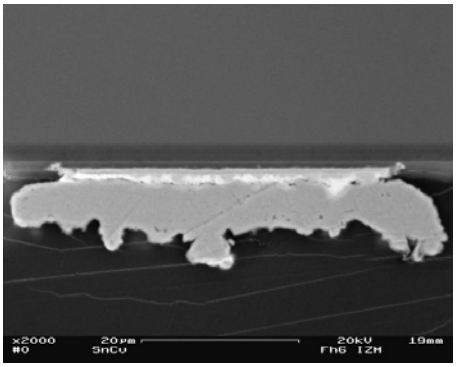

Fig. 12: Ultra thin contact with a Cu wiring on the bottom a thin layer of solder/intermetallic and a top Ni contact.

Lamination

Even though the chips are thin, lamination has be successfully performed without damage of the test vehicle chip. In first experiments the chips were laminated onto full area Cu-substrates. For different adhesive systems the lamination parameters where 30 kg/cm^2 with 190 °C for 3 minutes (epoxy resin, see figure 13) and 180 °C with 20 kg/cm^2 for 2 hours respectively (acrylic based glue).

Fig. 13: thin chip laminated with epoxy resin coated cover lay.

Contacting

Since the chips are flip chip bonded onto the flex substrate with a structured Cu wiring the contacting to other layers of the build up can be accomplished either by conventional through hole technique or by blind vias drilled with a laser.

Production Challenges and Cost Aspects

Embedding of passive as well as active components is highly attractive for miniaturization and increase of functionality. From the technological point of view it is an interesting and consequent combination of existing technologies and their exploitation. However, from a production perspective there are still many challenges. Technological issues such as yield, reliability, signal transmission losses, thermal management and test & quality standards are addressed in the above mentioned European development projects.

The implementation of embedding technologies requires a close cooperation among disciplines that had been formerly separated. The design of the electrical system including embedded passives and actives has different constraints and limitations. In this respect experts from technology and design have to cooperate closely. An exact translation of components which are surface mounted at present into exactly the same type as an embedded component is neither required nor necessary in most cases. Appropriate design tools are under development but do so far not offer easy drop in solutions for embedded components.

Also the cooperation among different contributors in the production chain will be more important. Today a processed chip from an IC foundry is likely to pass many processing steps before it is finally mounted and connected to a board surface. Chip layout and surface finishes are adapted to the requirements of conventional interconnection and packaging technologies. On the other hand PCB manufacturers have developed processes and materials for complex wirings in single or multiple layers. Both the packaged chip or component as well as the PCB are brought together only in the final assembly process. The future challenge is to adapt chip designs and finishes such that they are compatible with processes at the PCB manufacture. The PCB manufacture in turn has to address handling issues of ICs, positioning, interconnection and testing which at present is not within the common technology portfolio of a PCB manufacturer. The implementation of the respective equipment (die bonder, thermode bonder), the teaching of the involved employees and required ramp up of the new technologies would be the investment for the PCB manufacturer. For high end PCB manufacturers where the technical infrastructure such as clean environment (not necessarily clean room) and laser structuring is common the equipment cost will be low.

The final cost for a board containing embedded components is strongly dependent on the type of the embedded component that replaces an otherwise surface mounted device. It has been shown, that the board cost with embedded passives can be reduced by a factor of 50 %. Since rework of embedded components is not possible a high yield is essential for a realistic scale production process. Obviously the inclusion of active devices requires even stronger efforts in the process control.

Conclusions

It has been shown that embedding of active and passive devices into the printed wiring is possible with technologies that for the most part are available at a PCB manufacturer with a yield perspective that makes it reasonable for scale production. Additional equipment required for the presented technologies is limited. To realize all possibilities for embedding of components into the wiring board some of the system boundaries (i.e. between design and process technology and between the IC foundry and packaging) in the production chain of electronic equipment need to be broken down.

The use of embedded highly integrated systems was queried in the past. But market trends and novel applications has in the past been a persistent driver for such technology developments and is expected to be so in the future.

Acknowledgements

The authors would like to thank the European Union for financial support of this work in the framework of the projects HIDING DIES (IST-STREP-2002-507759) and SHIFT (IST-IP-2002-507745).

References

1. Ulrich R. K. and Schaper L. W. editors. Integrated Passive Component Technology. Hoboken, NJ: IEEE Press, Wiley-Interscience, 2003
2. Palm P., Touminen R., and Kivikero A., Integrated Module Board (IMB); an Advanced Manufacturing Technology for Embedding active Components inside organic Substrate", The 54th Electronic Components and Technology Conference, Las Vegas, USA, 2004, s28 p3
3. Aschenbrenner R., Ostmann A., Neumann A., and Reichl H., Process Flow and Concept for Embedding Active Devices. EPTC 2004, Singapore, 2004.
4. A. Ostmann, A. Neumann, J. Auersperg, C. Ghahremani, G. Sommer, Aschenbrenner R., and Reichl H., Integration of Passive and Active Components into Build-Up Layers, EPTC 2002, Singapore, 2002.

5. Fritz D., Sawoska D., and Durso F., Performance of Plated Additive Resistors, IPC/FED International Conference on integrated passive Components, Munich, Germany 2004.
6. Walther G., Tolerance Analysis of Ohmega-Ply Resistors in Multilayer PWB Design, CiruiTree, March 2001, http://www.circuitree.com/CDA/ArticleInformation/features/BNP__Features__Item/0,2133,21451,00.html
7. Chinoy P., Langlois M., and Schemenaur J., High Ohmic Value Embedded Resistor Material, CiruiTree, March2002. http://www.circuitree.com/CDA/ArticleInformation/coverstory/BNPCoverStoryItem/0,2135,72413,00.html
8. Tuominen R. Kivilathi J.K., A novel IMB Technology for Integrating active and passive Components, 4th International Conference on Adhesive Joining & Coating Technololgy in Electronic Manufacturing, 18 – 21 June, p 269, Helsinki, 2000.
9. Ostmann A. Kriechbaum A. De Baets J., and Kostner H., Chip Embedding in Printed Circuit Board Production, IMAPS-Nordic, fall 2005, to be published.
10. For information on HIDING DIES refer to: http://www.hidingdies.net/
11. For information on SHIFT refer to: http://www.vdivde-it.de/portale/shift/default.html
12. Löher T., Pahl B., Huang M., Ostmann A., Aschenbrenner R., and Reichl H., An Approach in Microbonding for ultra fine Pitch Applications: Technology and Metallurgy, The 7th VLSI Packaging Workshop of Japan, Kyoto, 2004.

Biographies

Thomas Löher is research scientist at Center Research Center of Microperipheric Technologies at TU Berlin since 2002. He is responsible for the passive and active embedding in the European project SHIFT. His expertise is in interface physics and chemistry, material sciences (semiconductors, metals). Recently he focuses on the integration of passive and active components into printed wiring boards. He studied physics at Technical University (TU) Berlin and received doctor degree in physical chemistry from Freie University (FU) Berlin in 1995.

Alexander Neumann graduated in micro system technology at University of Applied Science (FHTW) in Berlin in 2001. In the same year he joined the Research Center of Microperipheric Technologies at TU Berlin. His focus is on chip in board technologies and development of the Chip-in-Polymer processes such as laser structuring and laser drilling, metallization and lamination.

Lars Boettcher currently is a R&D engineer at Fraunhofer Institute for Reliability and Micro integration (IZM) Berlin. He specializes in wafer level processes with emphasis on chemical metallization technologies, photolithography and laser technologies for advanced packaging applications. Mr. Boettcher received an engineering degree from the university of applied science and business Berlin/Germany in 2000 in micro system technologies.

Barbara Pahl received M.S. degree in material science from Technische Universität Berlin in 1999. Since 2000 she is research scientist in the group “System Integration on Flex” at the Centre of Microperipheric Technologies at IZM and TU Berlin. Her major focus is on process technology and metallurgy of thin soldered contacts in ultra fine pitch thermode bonding on flexible substrates.

Andreas Ostmann has been with the Research Center of Microperipheric Technologies of TUB and the Fraunhofer IZM since 1992. He is head of the group Chemical Metallization and Advanced Printing and since 2003 also deputy head of the department Chip Interconnection Technologies. Mr. Ostmann is coordinator of the European project HIDING DIES. He received his diploma in Semiconductor Physics at the Technical University of Berlin (TUB) in 1991.

Rolf Aschenbrenner has been at the Fraunhofer Institute Reliability and Microintegration Berlin (IZM) since 1994 where he is head of the department Chip Interconnection Technologies and Deputy Director of the Institut. Rolf Aschenbrenner is currently Technical Vice President of the IEEE/CPMT society and he is board member of IMAPS-Germany. He received the diploma degree in physics from the University of Gießen, Germany, in 1991.

Herbert Reichl is author and co-author of more than 400 papers and many books. His work actually focusses on simulation methods and technologies for interconnection of microelectronic systems. Herbert Reichl is director of the Fraunhofer Institution for Reliability and Microintegration (IZM), Berlin. Since 1988 he is professor and head of the “Research Center of Microperipheric Technologies“ of the Technical University, Berlin. He joined the Fraunhofer Institute for Solid State Technology in 1971. His work focussed then on semiconductor sensors for temperature, pressure and humidity. Herbert Reichl received a doctor degree in electrical engineering at Technical University Munich in 1970.