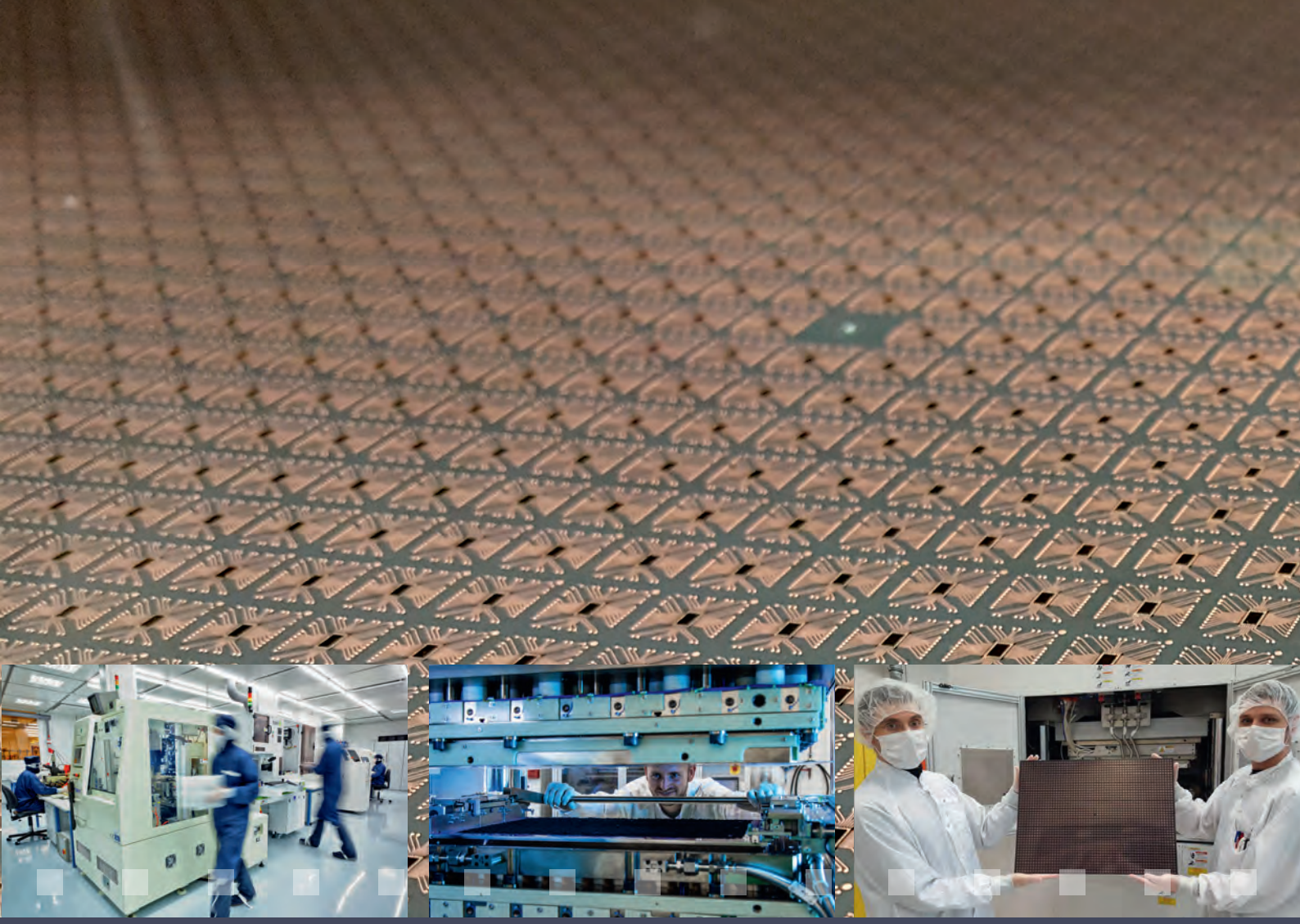


White Paper on Panel Level Packaging Consortium

by Tanja Braun, Michael Töpper, Rolf Aschenbrenner, Klaus-Dieter Lang

Fraunhofer Institute for Reliability and Microintegration IZM
Berlin, Germany

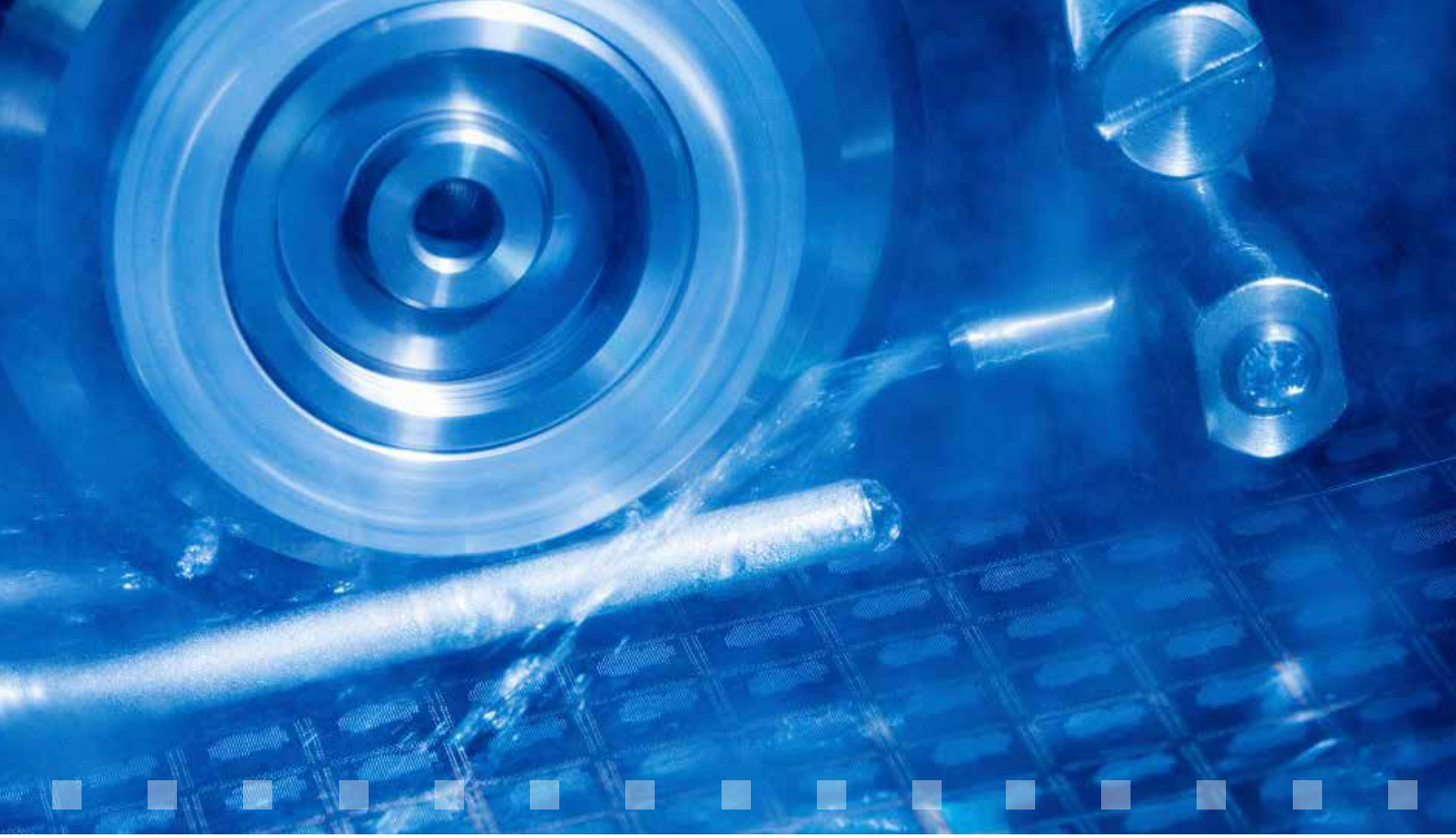
Fraunhofer IZM

Panel Level Packaging CONSORTIUM

White Paper

If you want to be kept up to date, please send an email to plp@izm.fraunhofer.de.

Fraunhofer Institute for Reliability and Microintegration IZM
2016



Content

1 Vision and Rational for Panel Level Packaging Research

Vision

Embedding die technology has its roots in the chip-first technology of GE developed for special applications 40 years ago mainly by Ray Fillion. Over the last decade it has developed into two types: Embedding into PWB (embedded die) and reconfigured molded wafer. FOWLP (Fan-Out Wafer Level Packaging) has been established as one of the most versatile packaging technologies in the recent past and is already accounting for a market value of over 170 million USD due to the tremendous increase in hand-held applications. The technology combines high performance, increased functionality with a high potential for heterogeneous integration and reduce the total form factor.

FOWLP has started in volume for mobile and wireless applications (mainly wireless baseband) and is now moving to automotive and medical applications. Infineon started with a 77 GHz Radar IC Chip Set (RASICTM). RTN7735PL and RRN7745P are the first 77 GHz solutions based on an eWLB package instead of a bare-die. They form a scalable platform comprising a three-channel transmitter and a four-channel receiver to build long- and mid-range system.

Today the FOWLP is dominated by wireless baseband SoC, but this will broaden to a broader product portfolio (Figure 1).

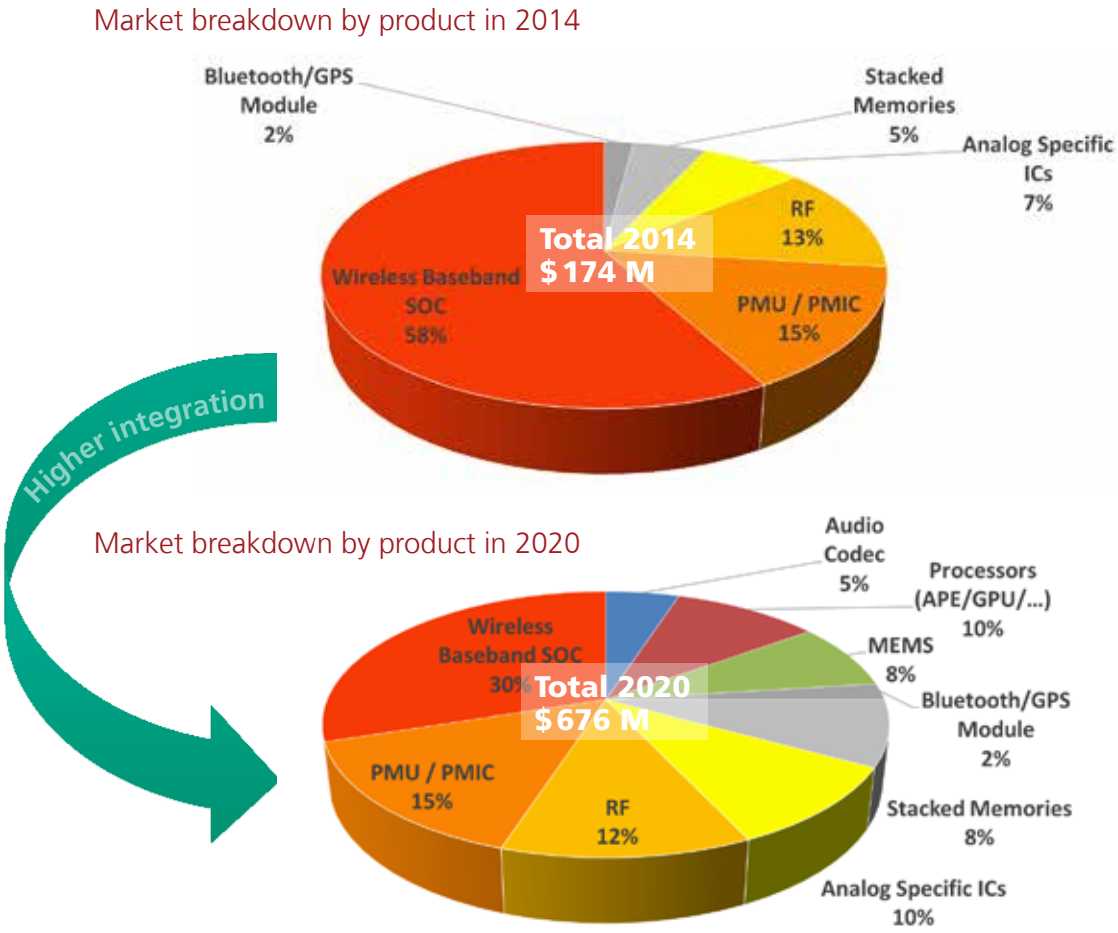


Figure 1: Breakdown by product type and evolution (Yole 2015)

Most standard packages for wireless are WB/FC-BGA but the costs are increasing with the growing number of I/Os due to organic interposer cost. In the near future FC-BGA substrates will have to go to 12/12 µm lines and space to keep the necessary routing density. TechSearch International has recently published the FC-BGA substrate trends (Figure 2):

CHARACTERISTIC	CURRENT (2014)	FUTURE (2014-2016)
Ball Count Rage	Up to 4,900	Up to 5,000
Body Size Range (mm)	Up to 71 x 71	Up to 72x72
Typical Construction	Build-up, up to 8-2-8 layers	Up to 8-2-8
Line/Space (µm)	Min. 15/15 to 18/20 on build-up layers	12/12
Via/Pad Diameter (µm)	Min. 45/90 on build-up layers	< 45/90

Figure 2: FC-BGA substrate trends (TechSearch International 2015)

Especially the lines and space requirements are reaching the area of thin film processing. Comparing the routing density of the different substrate technologies it is obvious that 2 µm lines and space is of high importance (Figure 3):

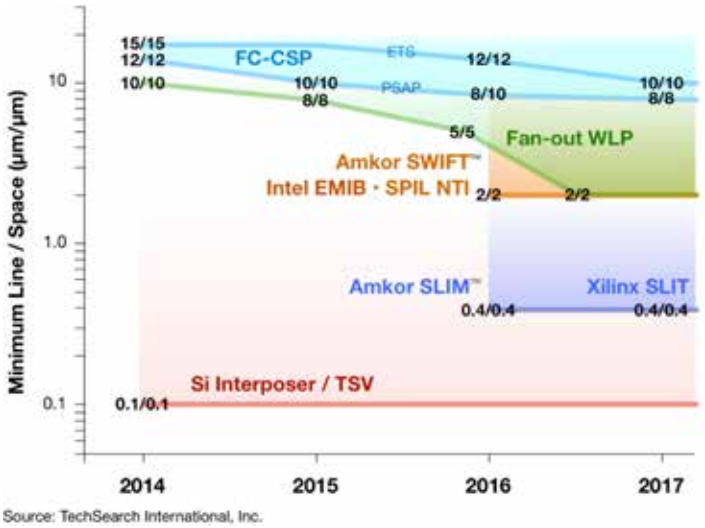


Figure 3: Comparison of Package Routing Densities (TechSearch International 2015)

The highest density can be reached in Si-Interposers due to high-end stepper lithography technology developed for FE-processing. Damascene-like processes might also be used for organic substrates in the future. Conventional WLP (fan-in type) is a substrate-less package but it is limited to a low I/O number due to the limited area for routing. Die size shrinkage is still a major barrier for FI-WLP keeping the BGA pitch constant. FO-WLP is therefore the optimal solution to keep track of these developments (Figure 4).

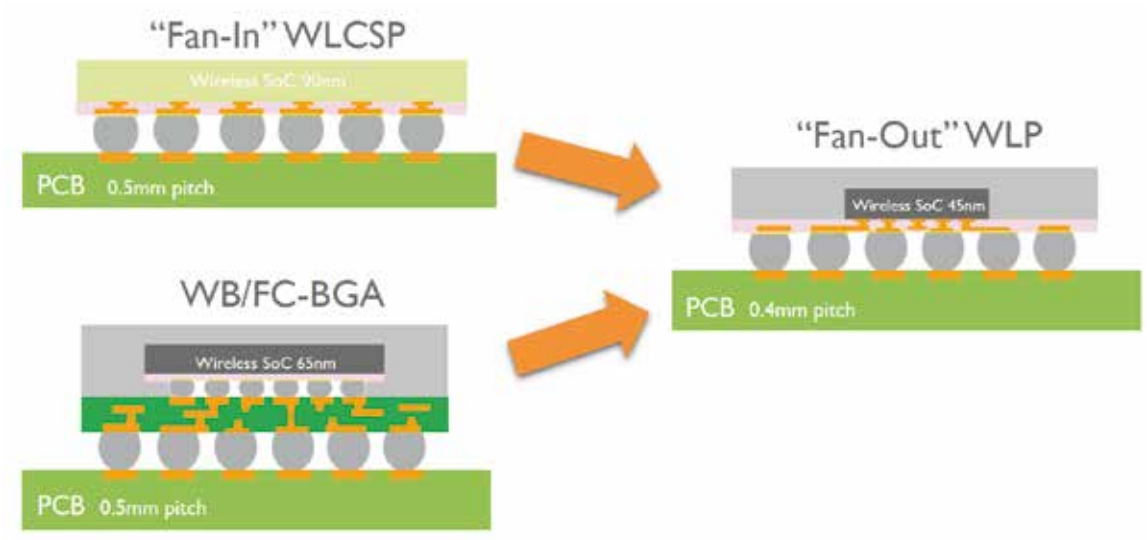


Figure 4: Comparison of FI-WLP, WB/FC-BGA and FO-WLP (Yole 2015)

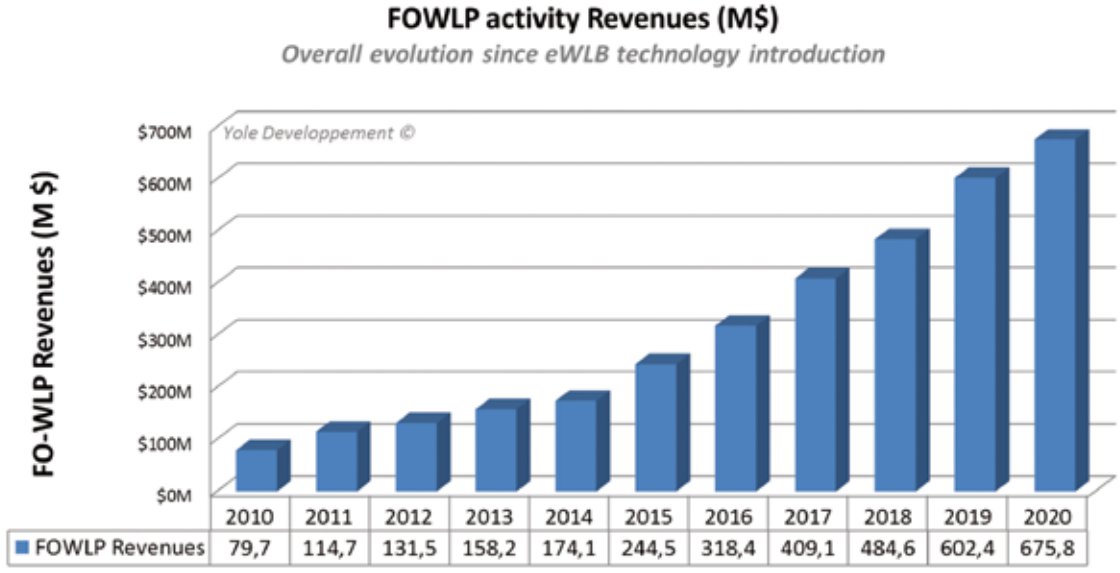


Figure 5: Proposed CAGR for eWLB (Yole 2015)

Cost reduction has been achieved by moving to 330 mm-technology and the move to panel level processing will push the technology further to lower cost. This can be viewed as a merge between the embedded die technology based on PWB infrastructure and the FOWLP on wafer level. The first being low cost by nature due to PWB technology but the supply chain is still complex because the PWB industry is not used to work with bare dies. Also the routing density is not fitting the WLP demands. Tight pad pitches require a redistribution of the dies before embedding ending up with higher cost for the total package. Therefore the first products have been power modules due to the possibilities of plating thick copper and the low number of I/Os of the IGBTs and MOSFETs. An additional advantage of the embedding die concept is the existing TPV (through package via) possibility which enables 3D packaging. In contrast to embedding die the FOWLP approach can use existing WLP equipment mostly installed at OSATs and some of the IDMs. Due to the higher resolution of the wafer lithography tighter pad pitches can be redistributed. Digital chip IC applications with a pin count of 100 to 250 are on the short term. Current limitations of the package size have to be extended for fully SiP including passive elements especially antennas to meet the needs of future packages. A wider range of dielectric materials for WLP enables the extension of FOWLP to RF-SiP. This is more difficult for PWB. Synergetic developments in materials and equipment are essential to guarantee high yield for this large expanding packaging technology. This proposal for a Panel Level Packaging Consortium should summarize the basic process technology steps for the move to large format. It should serve a value independent on several trademarks of commercial FOWLP types being sometime quite similar. It will help the OSATs to expand to large area manufacturing. Establishing partnerships which enables new technology developments are important. Equipment manufacturers form the PWB need to work with fabless and IDMs to adjust their tools for SiP requirements.

Rationale

Prime motivation for starting this PLPC at Fraunhofer IZM is the broad technology experience in wafer level packaging and substrate technology. Wafer level packaging has expanded to TSV technology which has offered the possibility to reload the MCM-D concept to SiP for advanced systems. Extension to larger wafer size is currently limited to 300 mm size and the next step may be 450 mm being delayed to unclear equipment roadmaps. But thin film processing has also developed to large panel formats for photovoltaic modules and displays. Therefore lithography with resolution down to 2 µm is available for large formats. On the other hand dimensions on the PWB are constantly decreasing. Embedding chips has opened the possibility to SiP. FO-WLP on panel size is now seen as the optimal synergy for SiP with high performance keeping the cost at a reasonably low level (Figure 6):

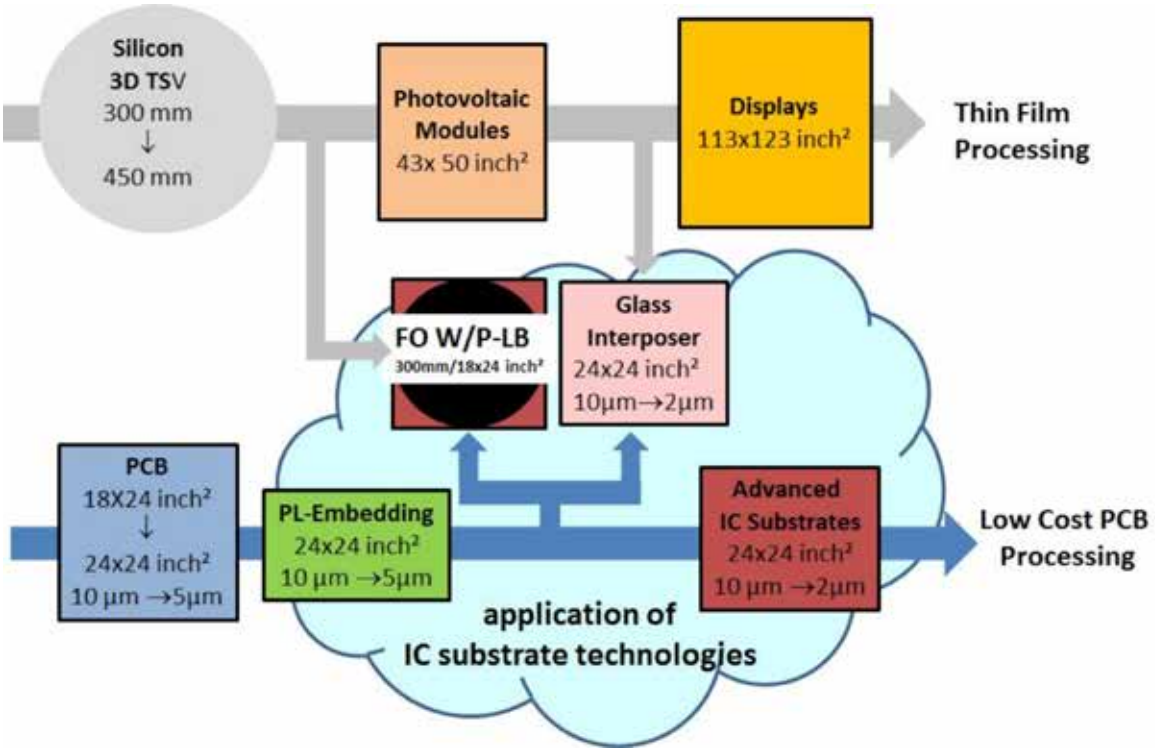
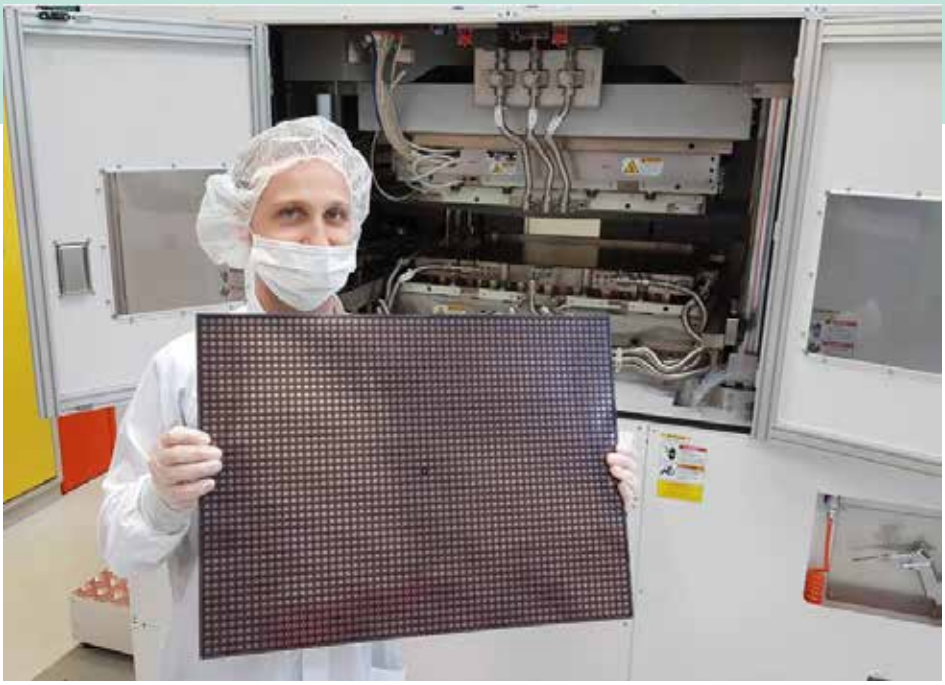


Figure 6: Comparison of thin film processing infrastructure with PWB

A very important reason for this consortium is the package IC co-design for FOWLP. Consequent serial IC design cannot guarantee highest performance due to the lack of knowledge including the package restrictions. Especially for RF chips the co-design is necessary to take package parasitic into account.

In summary the advantages of the proposed Panel Level Packing Consortium are:

- Electrical Performance: Proof of concept for RF-modules beyond 30 GHz
- Improved wiring and I/O: There is several decades of experience in fine line wiring and interconnection technology in the IC industry that can be leveraged for packaging technology
- Standardization: Standardization is key for embedding die package to multi-sourcing
- Definition of supply chain: The responsibilities from supplier to supplier are not yet defined compared to standard WLP technologies
- Thermo-mechanical reliability: Improved reliability compared to FI-WLP due to additional plastic packaging
- Cost: Cost advantages are perceived with the ultra-miniaturized approach proposed when coupled with large area, high throughput and high volume production



2 Previous WLP and Panel Level Research

Fraunhofer IZM was founded 1993 out of an R&D institute of Berlin's Technical University, that had already worked in advanced packaging since 1987. Fraunhofer IZM is a centre for highly robust technologies used for system integration. For 20 years the focus has been on high density substrates using Si, Glass and organic substrates as base materials. A fully equipped wafer processing line for Si wafer and glass wafer sizes between 100 und 300 mm for prototyping is available as well as a full panel level line for substrates up to 18" x 24". This WLP technology has been expanded over the last years to 3D integration using through substrate via processing.

IZM Wafer Level Packaging Line (RDL) for Wafer Sizes 100 mm / 150 mm / 200 mm / 300 mm

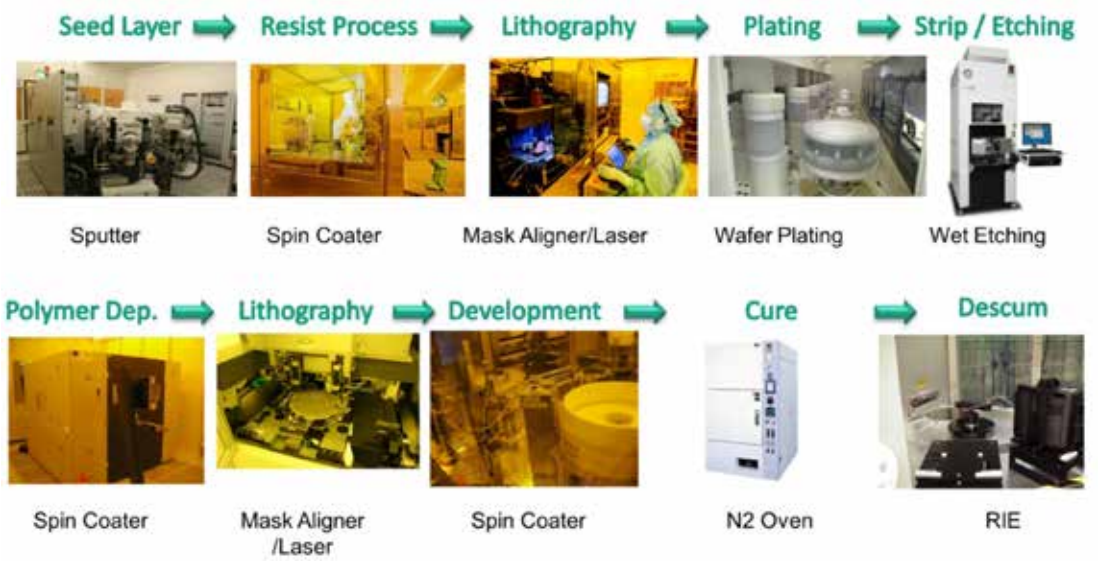


Figure 7: Wafer Level Line

In total Fraunhofer has invested several million euros to install a complete new and state-pf-the art panel level processing line:

IZM Panel Level Embedding Line from Wafer Scale to Panel Scale 610 x 456 mm² / 24'' x 18''

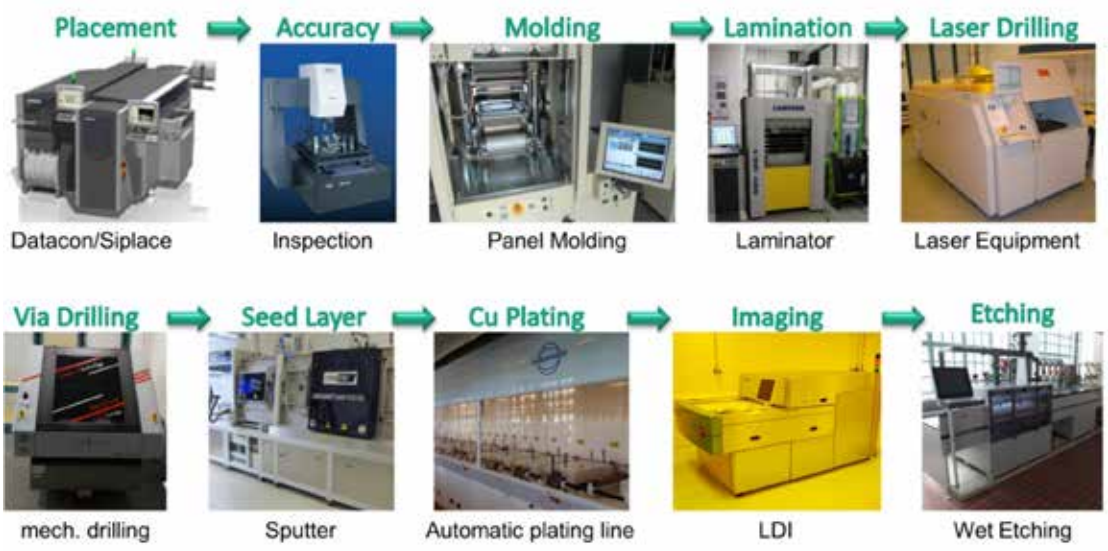


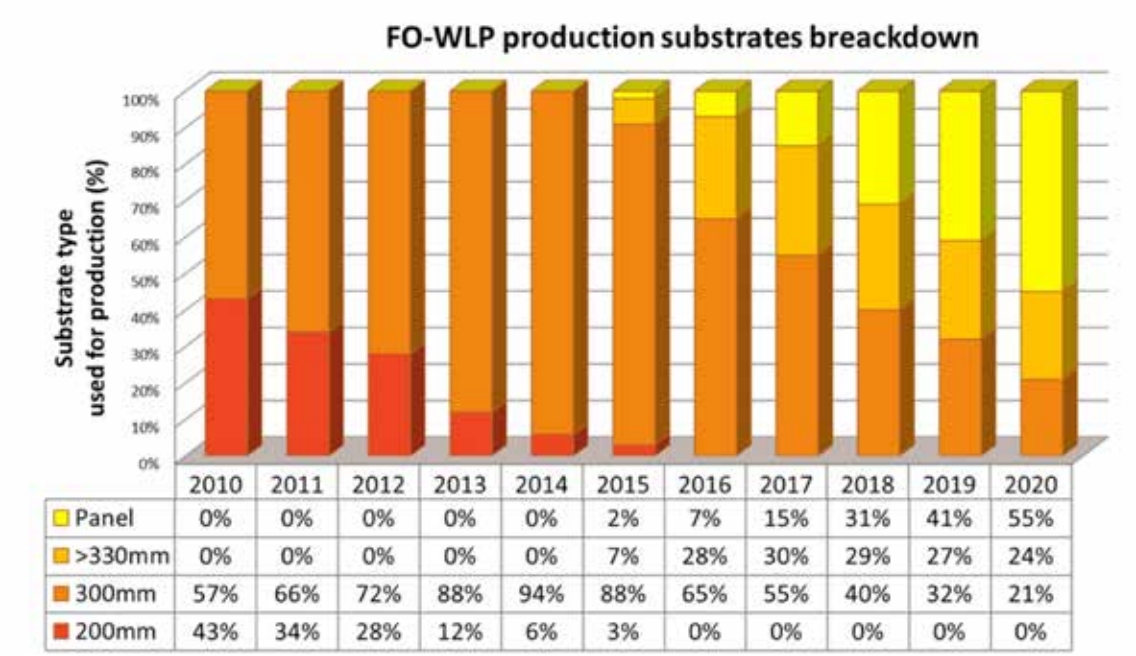
Figure 8: Panel Level Line

Teachearch International has just recently published a list of the ongoing R&D on FO-WLP on panel size (Figure 9)

COMPANY	PACKAGE BODY (mm)	MINIMUM L/S (µm)	PANEL SIZE (mm)
Amkor/J-Devices	12x12	20	320x320
ASE	6.3x4.7	15	510x410
Deca Technologies	6x6 to 12 x12	8 (5 engineering)	300
FCI/Fujikura	6.5x5.5	10 (RDL); 30 (substrate)	250x350
Fraunhofer IZM	–	20 (10 possible)	610x456
SPIL	9x9	≤10	370x470

Figure 9: FO-WLP Panel Sizes under development (TechSearch International 2015)

Different sizes for the panel are under consideration by different companies. Fraunhofer IZM is currently the only research institute working on this topic and is therefore the perfect location for such a consortium.
In addition Fraunhofer is already working in a couple of R&D projects to explore panel level packaging in conjunction with thin film processing. Yole is already proposing a market share of over 50 % for panel processing for FO-WLP in 2020 (Figure 10):



	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Panel	0%	0%	0%	0%	0%	2%	7%	15%	31%	41%	55%
>330mm	0%	0%	0%	0%	0%	7%	28%	30%	29%	27%	24%
300mm	57%	66%	72%	88%	94%	88%	65%	55%	40%	32%	21%
200mm	43%	34%	28%	12%	6%	3%	0%	0%	0%	0%	0%

Figure 10: FO-WLP production carrier breakdown till 2020 (Yole 2015)

Such a large market share in only 5 years can only be reached by a joint R&D effort bringing together equipment and material suppliers with the system designers of the FO-WLP-SiPs. Prime goal is to drive panel level FO-WLP to a similar performance as WLP but at lower cost (Figure 11).

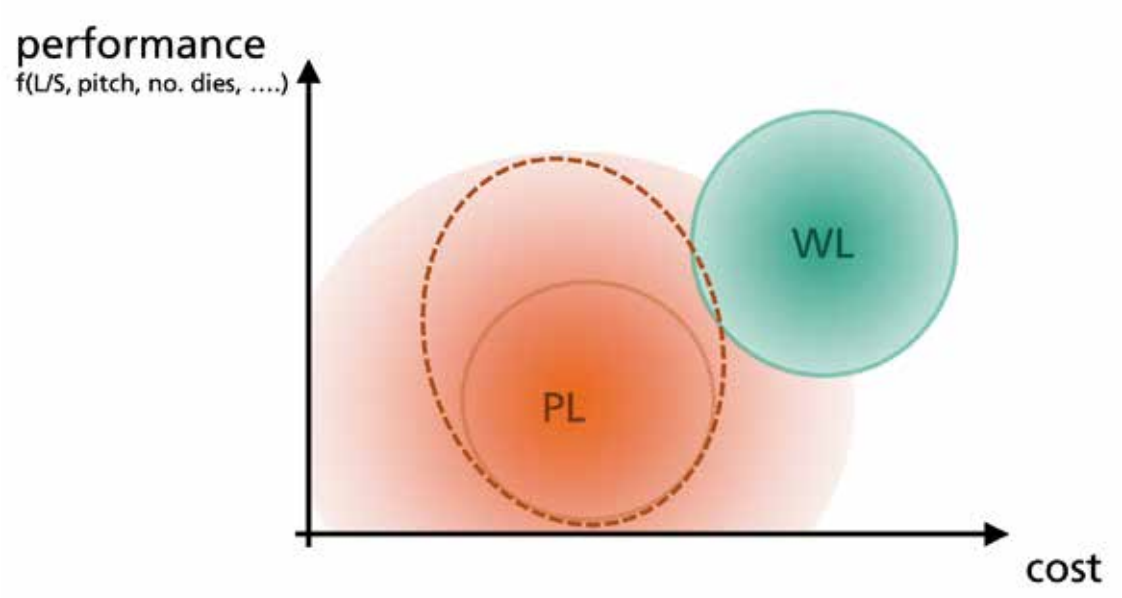


Figure 11: Panel-Level FO-WLP vs WLP

3 Research Organization and Project Description

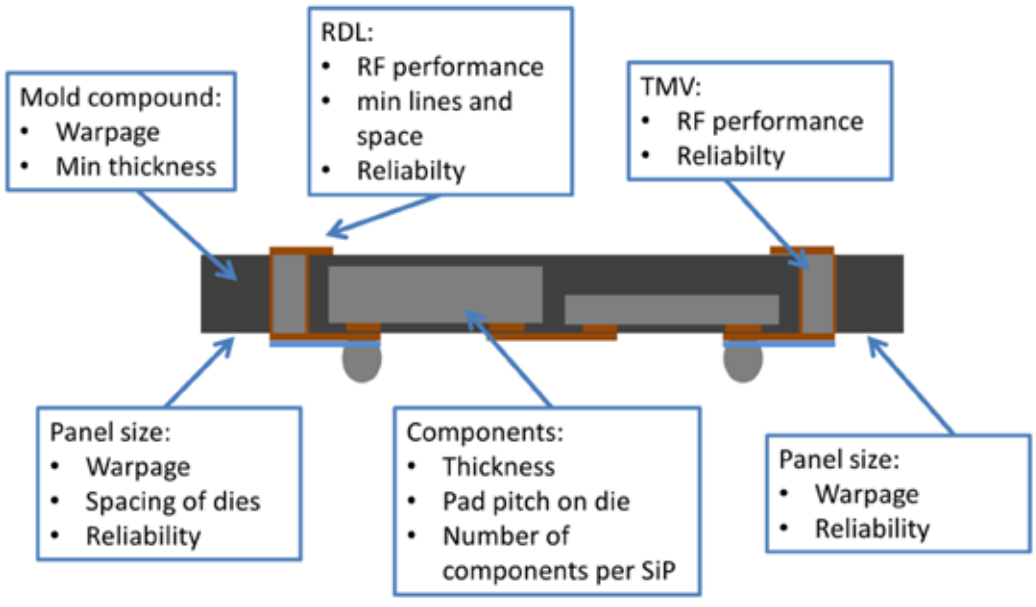


Figure 12: Focus on the R&D of the panel level packaging consortium

The team of Fraunhofer IZM will consist of highly experienced R&D engineers.

In the first phase of this consortium, the primary focus is on fundamental building block technologies, culminating in the design and build of one or more technology demonstrator vehicles:

- Warpage (>> Assembly, Manufacturability)
  - > Heterogeneous materials and non-symmetric structure cause bow
  - > Polymer materials with adapted CTE& modulus and low shrinkage are required
  - > Optimized layer sequence and design required
- Accurary/Resolution (>> Miniaturization)
  - > Improved optical recognition systems for placement equipment
  - > Imaging with high depth of focus and high resolution
  - > Local alignment >> LDI or scanner or stepper
- Yield (>> Cost)
  - > Suited materials and components
  - > Optimized processes
  - > Production experience >> learning curve
- Low k Polymers for RDL (>> Performance)
  - > Standard epoxy polymers are not sufficient for high performance RDL
  - > Low k with low loss are essential for RF performance
  - > Dry-film polymers offer the possibility for thick polymer layer beneficial for RF

The following challenges will be focused on and divided into different thrusts (Figure 13).

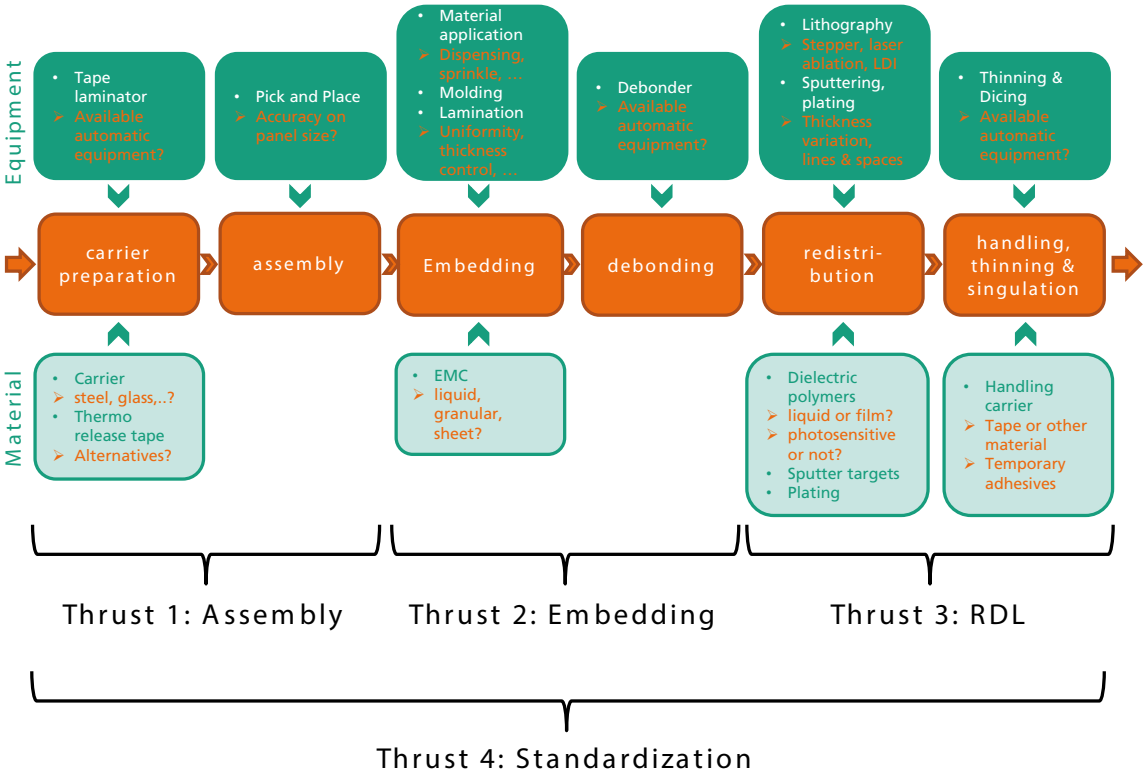


Figure 13: Challenges of panel level packaging and project organization into different thrusts

To solve the different interactions of the panel level packaging aspects the goal is to have a consortium consisting of Fraunhofer IZM and partners along the value chain including end users and manufacturing houses (OSATs) with the following tasks and targets:

- Fraunhofer IZM provides research excellence and PLP infrastructure
- End users defining future demands
- Equipment & material suppliers working on applied research for process industrialization and driving standardization
- OSATs working on process integration

Out of this process flow three main thrusts have been defined.

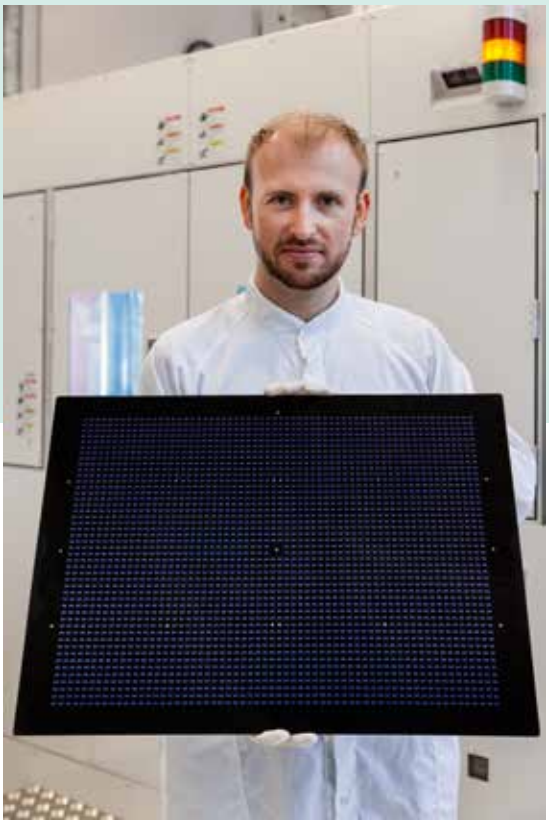
- Thrust 1: Assembly
- Thrust 2: Embedding
- Thrust 3: Redistribution Layer [RDL]
- Thrust 4: Standardization

The objectives, approaches and deliverables of the different thrusts will be described in the SoW (statement of work).

1st Year: Basic Panel Level Packaging Process

The research objective of this thrust is to explore, develop and demonstrate basic panel level process steps.

- Maximum package size
- Minimum of die shift for larger substrates
- Minimum die-to-die distance
- Minimum mold clearance distance
- Minimum die side size
- Package minimum thickness (w/o BGA)
- Maximum I/O count for BGA
- Maximum package size
- Minimum line and space for RDL
- Minimum warpage
- Low k and low loss polymers for RDL



PARAMETER	TARGET 1st YEAR	TARGET 2nd YEAR
Number of Components	2	5
Package size	12 mm x 12 mm	30 mm x 30 mm
Die-to-die distance	200 µm	100 µm
Frequency Range	1 GHz	30 - 80 GHz
Pad Pitch on die	200 µm	150 µm
Panel Size	18" x 12"	18" x 24"
Panel Thickness	350 µm	200 µm
RDL		
Line/space	10 µm / 10 µm	5 µm / 5 µm
tolerance	+/- 15 %	+/- 10 %
Number of layers	2	4
Dielectric thickness	10 µm	20 µm
Dielectric constant	3	2,5
Dielectric loss	< 0.01 @ 10 GHz	< 0.005 @ 30 GHz
Reliability	JEDEC standard, MSL per-conditioning (Level 2-3), 3 x Solder reflow at 260 °C, 500 cycles -40 to + 125 °C TC	JEDEC standard, MSL per-conditioning (Level 2-3), 3 x Solder reflow at 260 °C, 1000 cycles -40 to + 125 °C TC, HAST 121 °C, 85 % RH, 96 hrs
	Draft cost model	Complex cost model

The focus of this 1st year is to develop and apply design methodologies for the Panel Level Packaging Consortium with regard to signal and power integrity as well electromagnetic interference and electrical test.

2nd Year: Panel Package Integration Test Vehicles

The research objective of this thrust is to explore, develop and demonstrate ultra fine multilayer wiring on FOWLP substrate to overcome the barriers of current organic substrates. The focus will be on a RF-test vehicle which will be defined by the partner in the first year.

4 Industry Benefits and Membership Categories

Benefits

Fraunhofer IZM is a non-profit research organization creating an opportunity for a cohesive, comprehensive and interdisciplinary research program and team needed to cover the entire range of technologies in the panel level program. It has significant investments in state-of-the-art facilities for packaging and semiconductor design, materials, processes, fabrication, integration, assembly, test and reliability. This synergy brings significantly greater benefits to companies choosing to join the program, unlike other single-entity programs. Beyond the traditional research technology outcomes, members who actively participate in this program can expect opportunities to:

1. Leverage the company funding by more than an order of magnitude.
2. Couple their short term internal, competitive R&D within their company that typically covers up to about 3 years with the proposed pre-competitive 3-6 years ahead of the need at minimal cost.
3. Explore a variety R&D technology options made possible by the comprehensive Panel Level Packaging Consortium that are not possible with the available internal R&D investments within the company.
4. Mentor and shape research program directions.

5. Gain early access to leading-edge technologies via participation in monthly, quarterly, and annual program reviews, conference calls and secure member websites.
6. Co-author and co-present technical papers on mentored projects.
7. Possibility to assign an engineer on the campus of Fraunhofer IZM to actively participate to gain maximum benefit from the Panel Level Packaging Consortium.
8. Link supply chain companies for acceleration of product technology developments with end user companies.

Rules for Participation

All members will be informed regularly about the attained research results or work progress by Fraunhofer IZM and all members will get a copy of the final report summarizing all results of the project.

If required for the execution of the project and for the duration and implementation of the project only, the members shall grant each other a non-exclusive, non-transferable, non sublicensable, royalty free right of use to both already existing IPR and IPR generated or created during the performance of the project. Fraunhofer IZM will grant to all Full Consortium Members non-exclusive, royalty free licenses to all results and all IPRs generated and created during the performance of the project.

All members must be aware that FO-WLP technology is subject to various patents held by third parties. Fraunhofer IZM makes no warranty and provides no indemnity that the results and any licenses granted to Full Consortium Members do not infringe any third-party rights. Furthermore, Fraunhofer IZM liability with regard to the performance of the project will be restricted as usual within similar R&D activities.

Fraunhofer IZM is part of the mainly publicly funded non-profit Fraunhofer-Society. As all R&D activities will take part in Germany and will be done by German scientists German law will apply to any Consortium Agreement

Membership Categories

Two company membership categories are proposed: Full (Consortia), and Supply Chain Memberships (SCM). The cost and the benefits are significantly different. Full Consortia Members will enjoy all the benefits described above with rights to I/P across all R&D tasks for their fundamental research. Supply Chain Members (SCM) participate in meetings, and are involved in research projects as an active participant where their materials, services, and/or equipment are needed to achieve the project goals. The SCM's do not receive any IP rights, and will have limited visibility to program information.

5 Consortium Launch Schedule

The consortium launch is planned for 2nd half of 2016 based on a schedule of discussions and consulting with an International Advisory Board made up of industry leaders from Japan, Korea, Europe and US, generating a final executive summary to send to companies, identifying companies from around the world that are interested in joining the consortium and finalizing the initial research launch program based on the funds available from the initial set of companies.

Panel Level Packaging CONSORTIUM

Panel Level Packaging Symposium
Jun 28, 2016 - Jun 29, 2016

DAY 1, June 28, 2016
(open for everybody)

9:00 Introduction to Fraunhofer IZM – *Klaus-Dieter Lang, head of Fraunhofer IZM*
9:30 Keynote/Overview Panel Level Packaging – *Islam A. Salama, Intel Corporation*
10:00 Introduction Panel Level Packaging Consortium – *Tanja Braun*

10:30 Coffee Break

11:00 Assembly Strategies for Fan-out Panel Level Packaging – *Karl-Friedrich Becker*
11:20 Molding/Embedding for Fan-out Panel Level Packaging – Materials and Technologies – *Tanja Braun*
11:40 RDL for Fan-out Panel Level Packaging – Materials and Technologies – *Lars Böttcher/Markus Wöhrmann*
12:00 Discussion – *Moderator: Rolf Aschenbrenner*

12:30 Lunch

13:30 LabTour: Substrate Line • Cleanroom • Assembly and Encapsulation • Advanced Material Analytics

15:30 Coffee Break

16:00 Standardization Activities – *Walter Huck, Murata Europe*
16:30 Closing remarks – *Rolf Aschenbrenner*

19:00 Social Event with Berlin Flair

DAY 2, June 29, 2016
(only for companies who have signed the LOI or contract)

9:00 - 15:00
Topics: Introduction Members (10 - 15 min per partner)
Introduction Statement of Work (SOW)
Legal Aspects, IP Rules

Location: Fraunhofer IZM, Gustav Meyer Allee 25, 13355 Berlin / Germany

6 Published R&D Results and List of Public Funded Projects (Selection)

Published Results

[1] T. Braun, S. Raatz, S. Voges, R. Kahle, V. Bader, J. Bauer, K.-F. Becker, T. Thomas, R. Aschenbrenner, K.-D. Lang; Large Area Compression Molding for Fan-out Panel Level Packing; Proc. of ECTC 2015; San Diego, USA.

[2] T. Braun, K.-F. Becker, S. Voges, J. Bauer, R. Kahle, V. Bader, T. Thomas, R. Aschenbrenner, K.-D. Lang; 24”x18” Fan-out Panel Level Packing; Proc. of ECTC 2014; Orlando, USA.

[3] T. Braun, K.-F. Becker, S. Voges, T. Thomas, R. Kahle, J. Bauer, R. Aschenbrenner, K.-D. Lang; From Wafer Level to Panel Level Mold Embedding; Proc. of ECTC 2013; Las Vegas, USA.

[4] T. Braun, M. Bründel, K.-F. Becker, R. Kahle, K. Piefke, U. Scholz, F. Haag, V. Bader, S. Voges, T. Thomas, R. Aschenbrenner, K.-D. Lang; Through Mold Via Technology for Multi-Sensor Stacking; Proc. of EPTC 2012; Singapore.

[5] T. Braun, K.-F. Becker, L. Böttcher, A. Ostmann, E. Jung, S. Voges, T. Thomas, R. Kahle, V. Bader, J. Bauer, R. Aschenbrenner, M. Schneider Ramelow, K.-D. Lang; Potential of large area mold embedded packages with PCB based redistribution; Proc. of IWLPC 2011, Santa Clara, Ca., USA.

[6] T. Braun, K.-F. Becker, S. Voges, T. Thomas, R. Kahle, V. Bader, J. Bauer, K. Piefke, R. Krüger, R. Aschenbrenner, K.-D. Lang; Through Mold Vias for Stacking of Mold Embedded Packages; Proc. of ECTC 2011, Orlando, USA.

[7] T. Braun, K.-F. Becker, L. Böttcher, J. Bauer, T. Thomas, M. Koch, R. Kahle, A. Ostmann, R. Aschenbrenner, H. Reichl, M. Bründel, J.F. Haag, U. Scholz; Large Area Embedding for Heterogeneous System Integration; Proc. of ECTC 2010, pp. 550-556, 1.-4.6.2010, Las Vegas, NV, USA.

[8] M. Töpper, K. Hauck, M. Schima, D. Jaeger, K.D. Lang "A sub-4 µm Via Technology of Thinfilm Polymers using Scanning Laser Ablation" Proceedings IEEE ECTC 2015

[9] I. Ndip, M. Töpper "Fundamentals of Electrical Design and Fabrication Processes of Interposers, Including their RDLs" PDC Proceedings IEEE ECTC 2015

[10] M. Töpper, M. Wöhrmann, N. Jürgensen, I. Ndip, S. Takahashi, M. Takahashi, K. Kitaoka "Copper Filling of Through Glass Vias and Electrical Validation up to 110 GHz" GIT Workshop Atlanta 2013

[11] M. Töpper, Th. Fischer, T. Baumgartner, H. Reichl „A comparison of Thin Film Polymers for Wafer Level Packaging" Proceedings ECTC 2010, Las Vegas

[12] H. Reichl, R. Aschenbrenner, M. Töpper, H. Pötter
Heterogeneous Integration -– Building the Foundation for Innovative Products
More than Moore (Hrsg. G. Q. Zhang, A.j. van Roosmalen), Springer Verlag 2009, pp 279 – 303,
ISBN 978-0-387-75592-2

Funded Projects

[1] MST SmartSense, funded by German BMBF, in coop with Bosch, Aemtec, Binder Elektronik,…; Development of an e-compass based on conventional and FOWLP

[2] CAJAL 4EU, funded by EU/ENIAC, in coop with NXP, Bosch, Silex,…; Integration of an FOWLP packaged CMOS biosensor into microfluidics

[3] Smart-MEMPHIS, funded by EU/H2020, in coop with Silex, Acreo, Chalmers…; Development of piezo-MEMS based energy harvester with FOPLP

[4] InteGreat, funded by German BMBF, in coop with OSRAM, Würth, Mühlbauer,…; FOWLP and FOPLP of LEDs

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