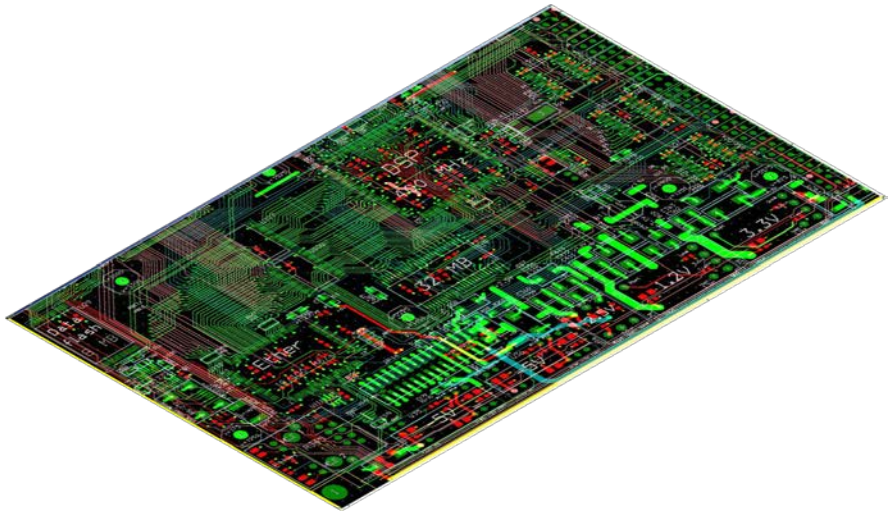
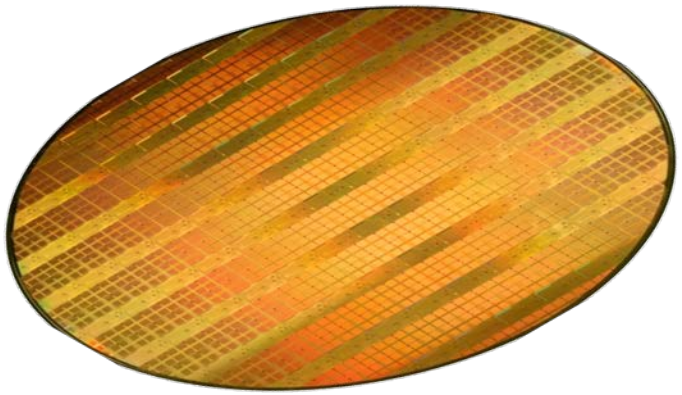
Dual Integration - Verschmelzung von Wafer und Panel Level Technologien

Dr. Michael Töpper
BDT



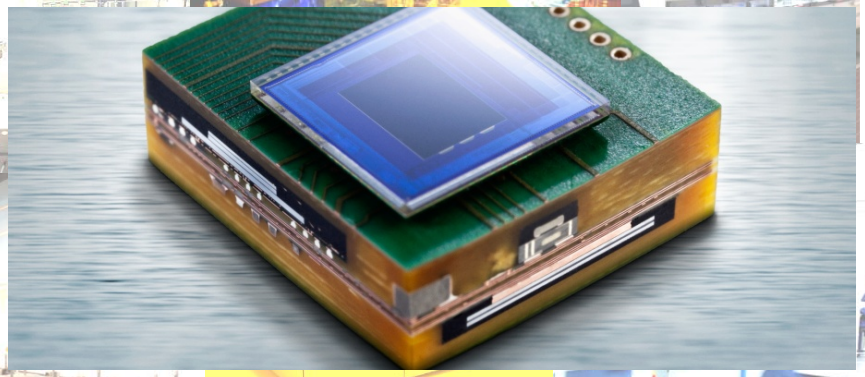


Introduction

Fraunhofer IZM

Introduction

Why do we need
such large machines
to build such small systems?



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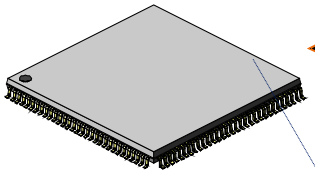
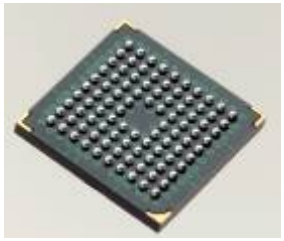
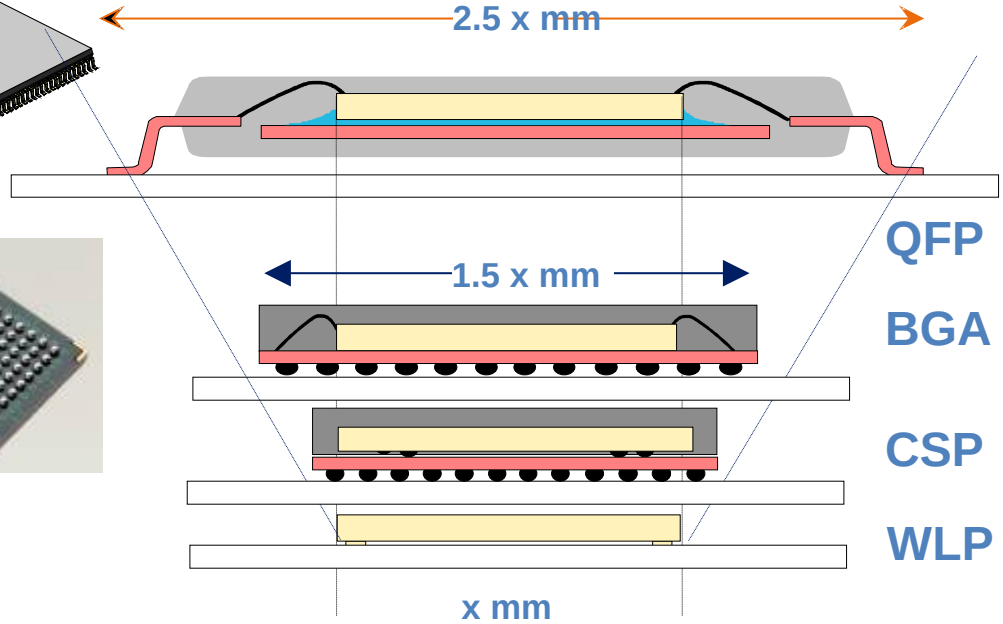
Introduction – Development of *Single Chip Packaging*





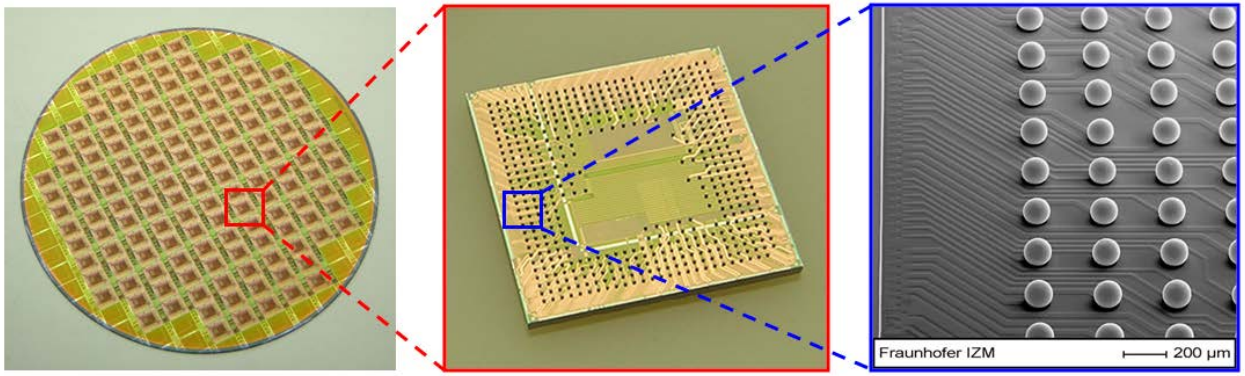


Package form factor

Package area / chip area

QFP	~ 5,5
BGA	~ 2.0
CSP	< 1.2
WLP (fan in)	= 1

Wafer Level Packaging WLP



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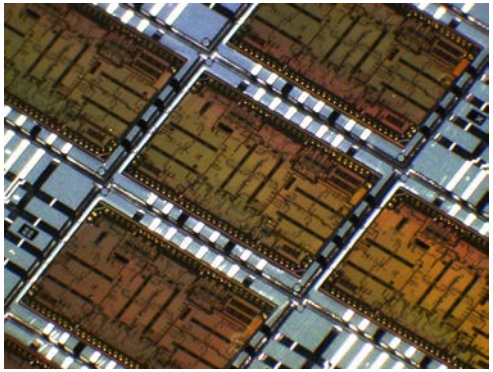
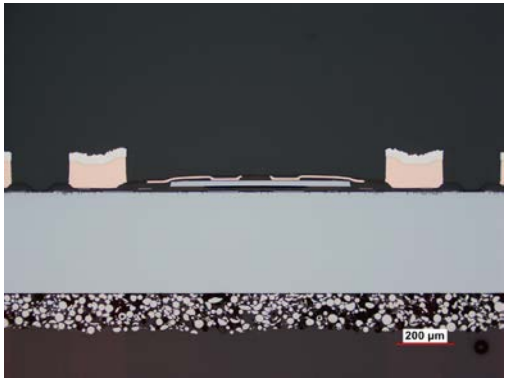
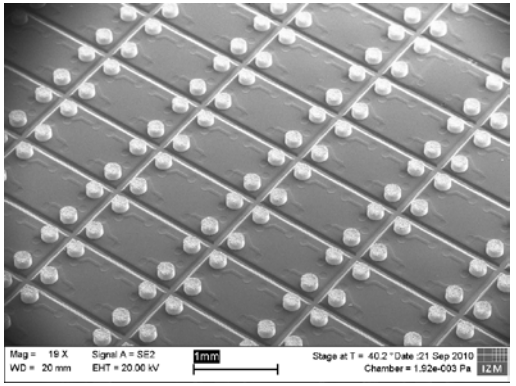
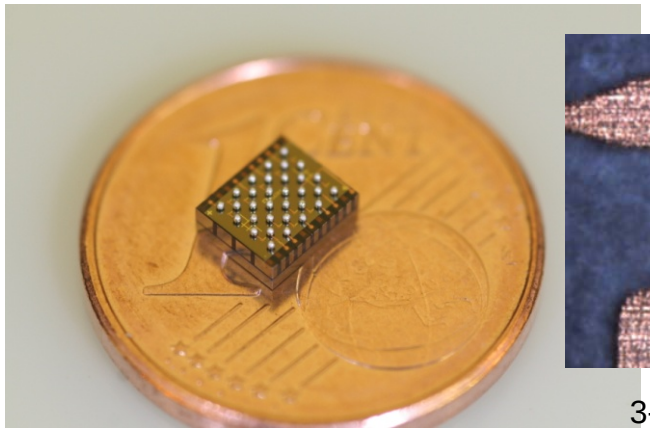
Example of WLP at IZM: Automotive Application



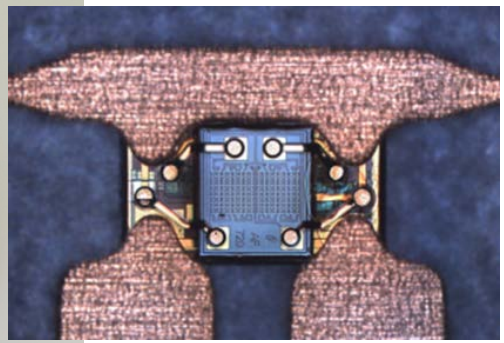




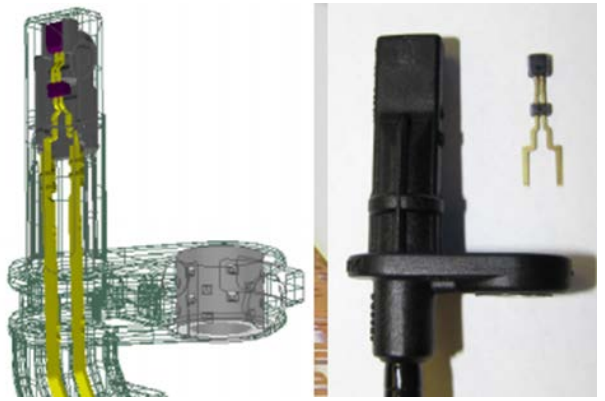
cross section of a three chip stack using chip embedding: thin chip embedded on wafer, formation of a RDL, Cu pillar



Bumped 3-D Stack



3-D Stack on leaddfram



Final Sensor in “DAG” Housing

Chip scale package integration of different microsystem technologies by thin die stacking, polymer embedding and redistribution/bumping for automotive applications

ESTLES

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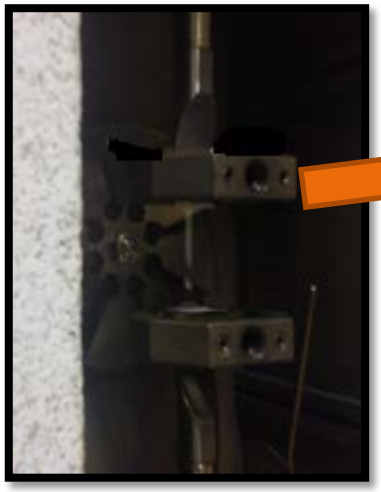
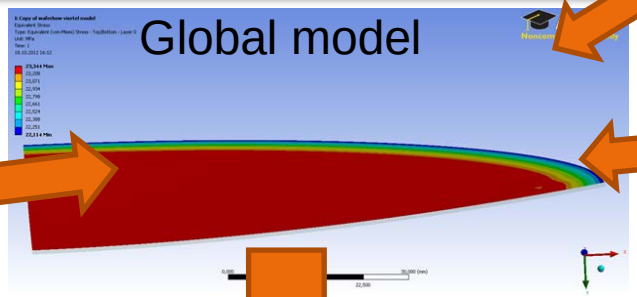
Reliability prediction is key (thermomechanical simulation) (Department: Environmental and Reliability Engineering)

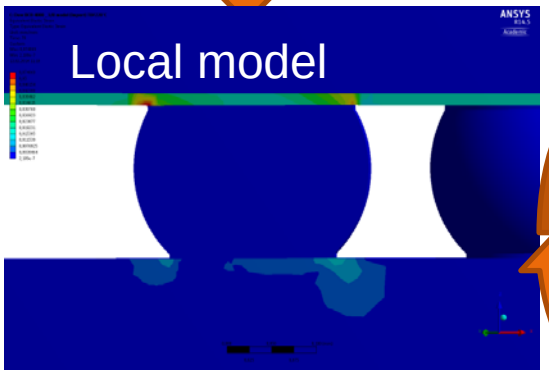
Free standing films



- CTE & Tg
- Elongation to break
- Youngs modulus
- Tensile strength

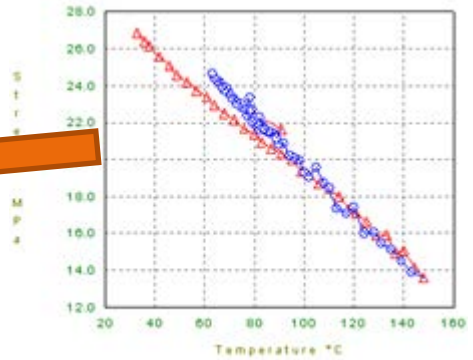
Verification of the stress and bow solution of the model
- Analytical solution
- Bow measurements



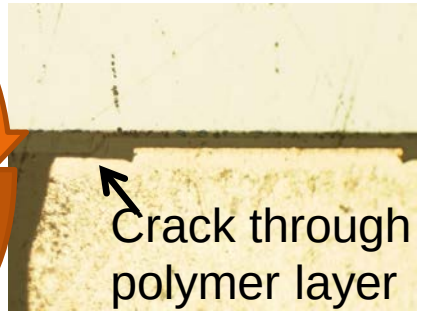


Stoney equation

$$\sigma_f = \frac{E_s d_s^2}{6(1-\nu_s)Rd_f}$$



Bow and stress measurement



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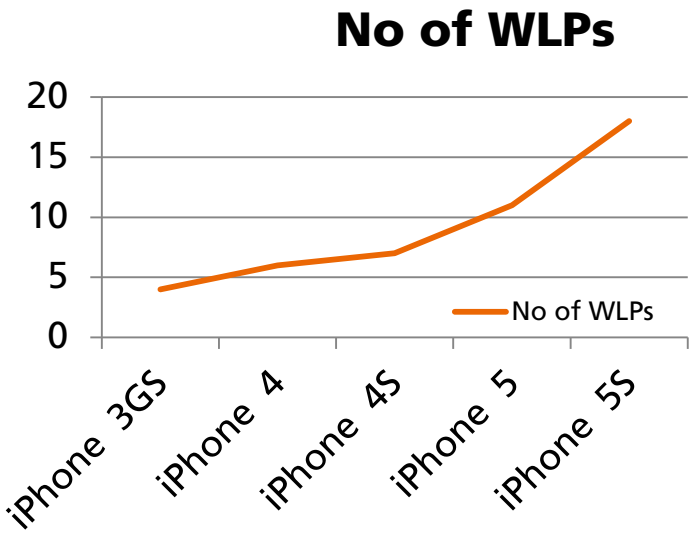
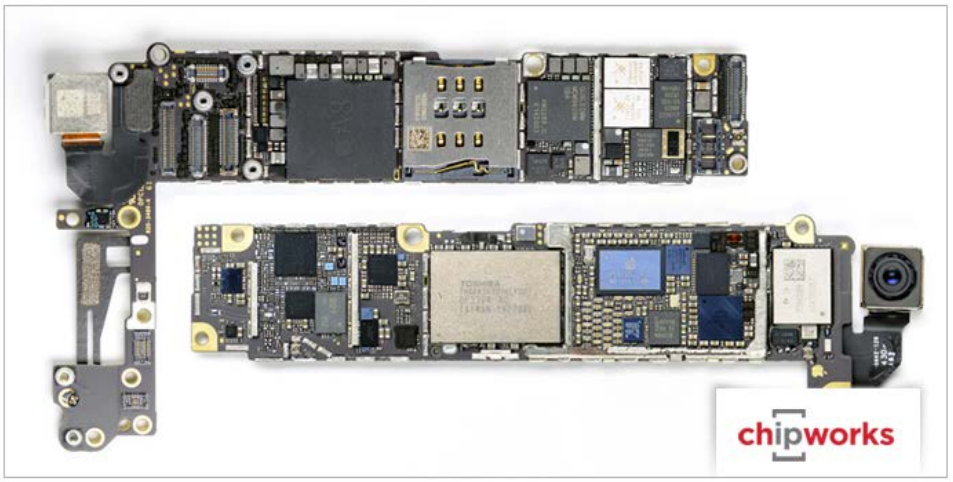
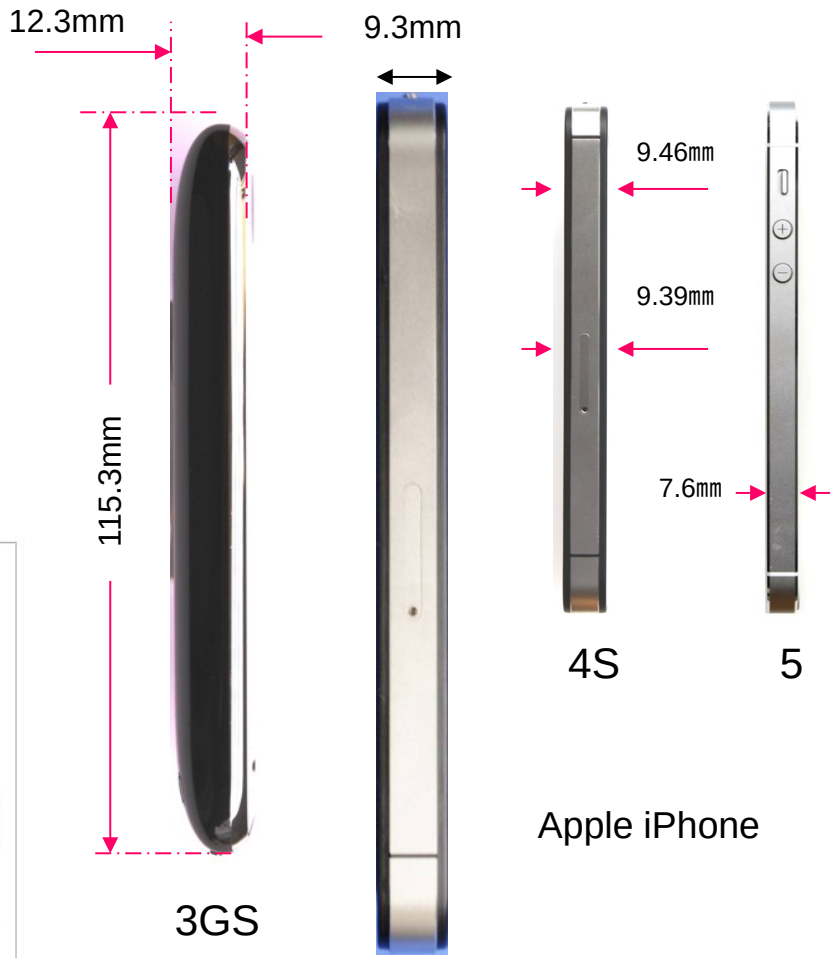
Wafer Level Packaging: Mainstream for Mobile Products







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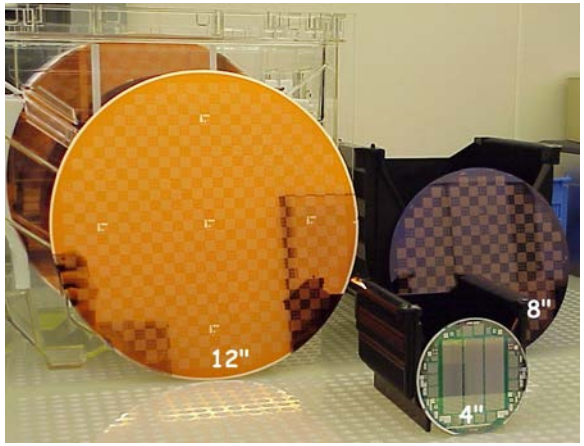
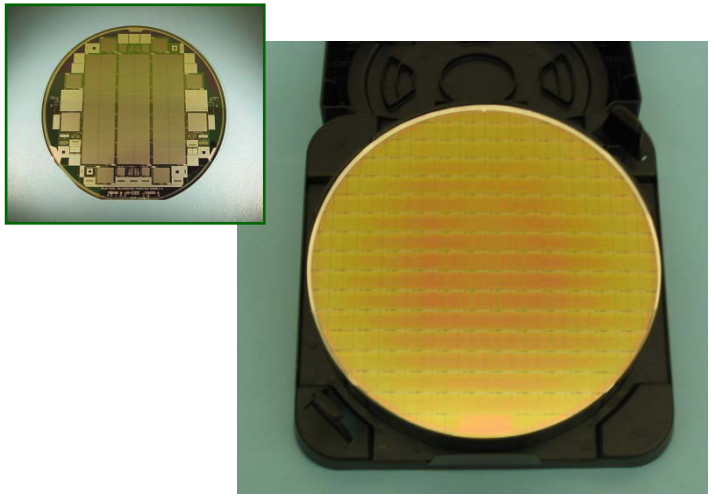
Wafer Level Packaging: Compatibility of Wafer Sizes is key

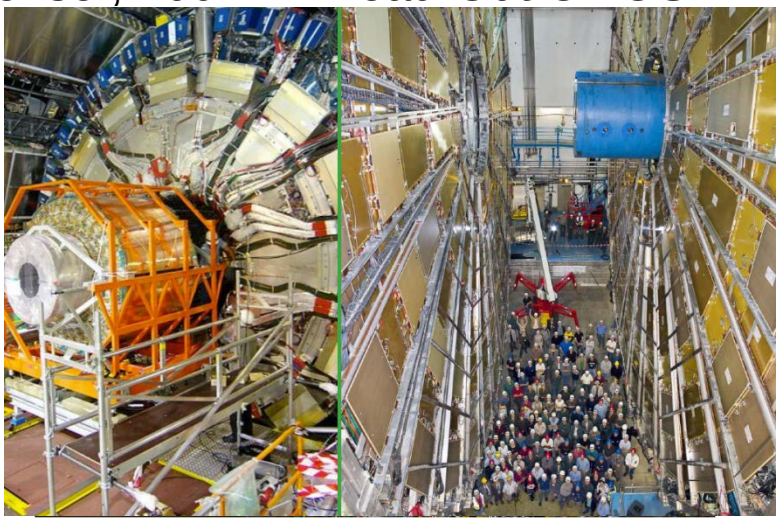


Sensors:	100 mm – 200 mm
ASICs:	150 mm – 200 mm
µProcessors:	200 mm – 300 mm
Memory:	300 mm
others:	single chips, wafer parts, …

Electronic Systems

Example ATLAS (CERN): 100 mm Sensor, 200 mm Read-Out CMOS





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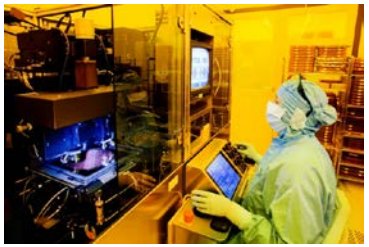
IZM Wafer Level Packaging Line (RDL)
for Wafer Sizes 100 mm / 150 mm / 200mm / 300 mm

Seed Layer → **Resist Process** → **Lithography** → **Plating** → **Strip / Etching**

Sputter

Spin Coater



Mask Aligner

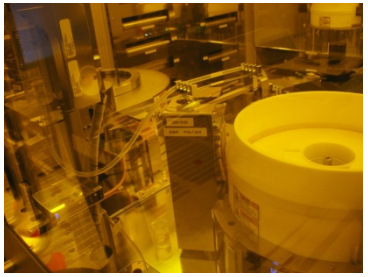
Wafer Plating

Wet Etching

Polymer Dep. → **Lithography** → **Development** → **Cure** → **Descum**

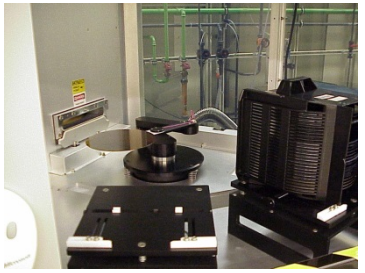
Spin Coater

Mask Aligner



Spin Coater

N2 Oven



RIE

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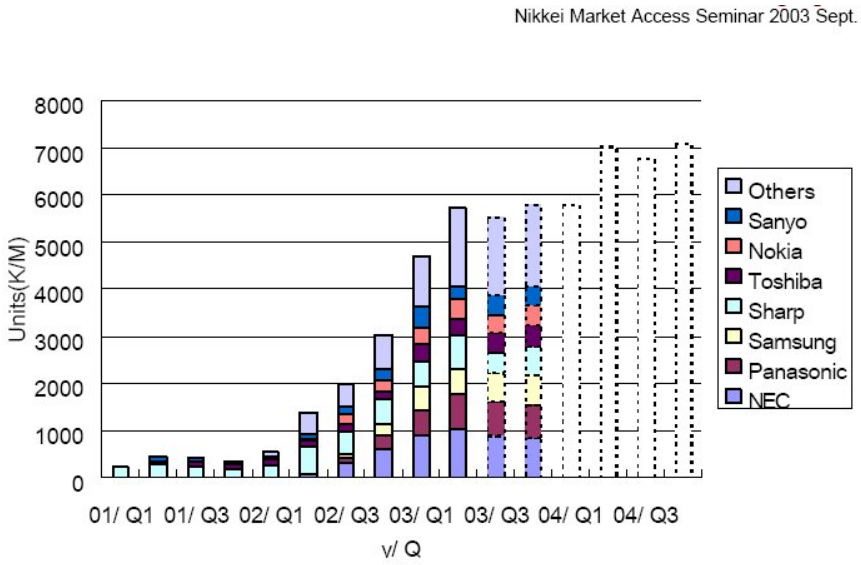
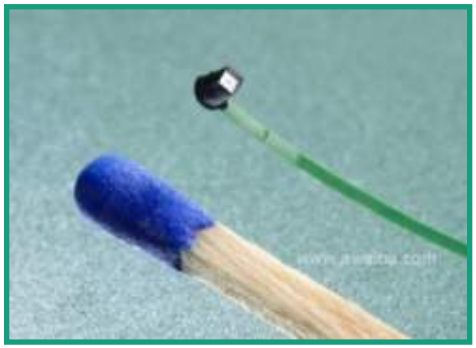
Question in 2003: Do we need a camera in a phone?

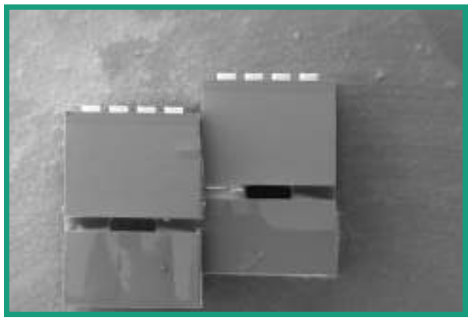


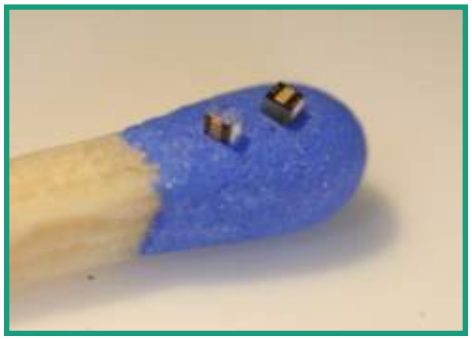
2014: Global smartphone shipments totaled 1.167 billion units in 2014

Extension of WLP to 3D Integration using TSV

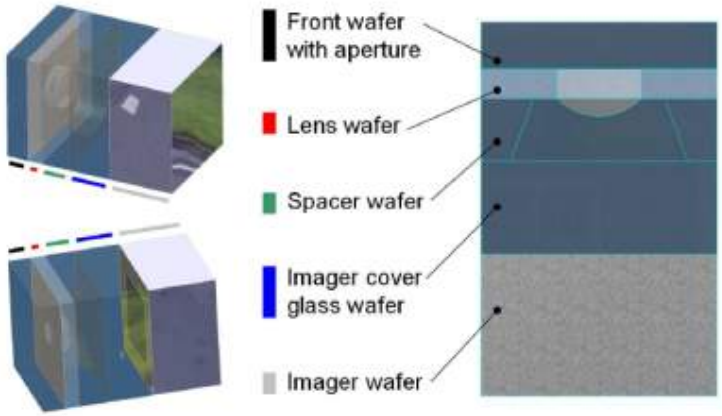
Wafer-Level-Cameras

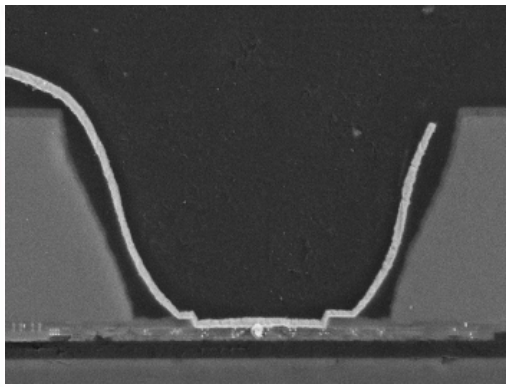






- Bringing the electrical contact to the back-side of the sensor
- Wafer level integration of optics and camera electronics
- Module size: 0.7 x 0.7 x 1.0 mm³
- Application: low-cost-endoscopes
- Partner: Awaiba GmbH





AWAIBA

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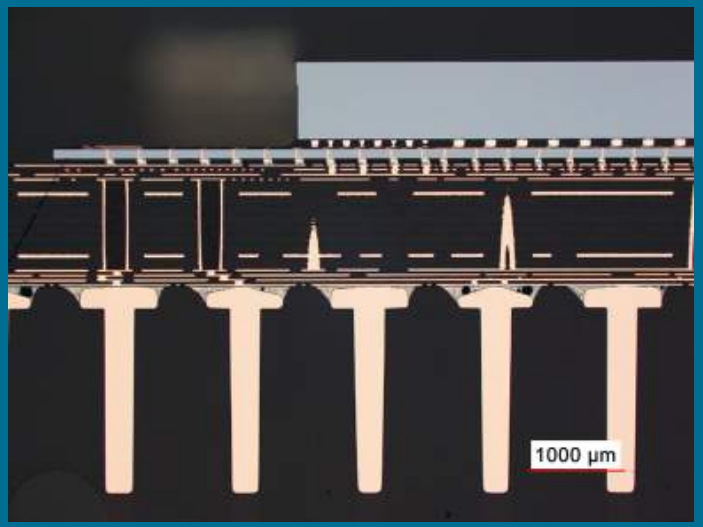
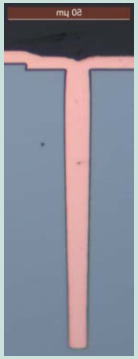
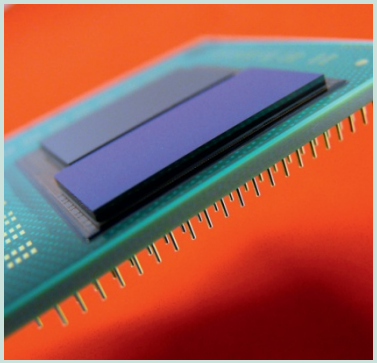
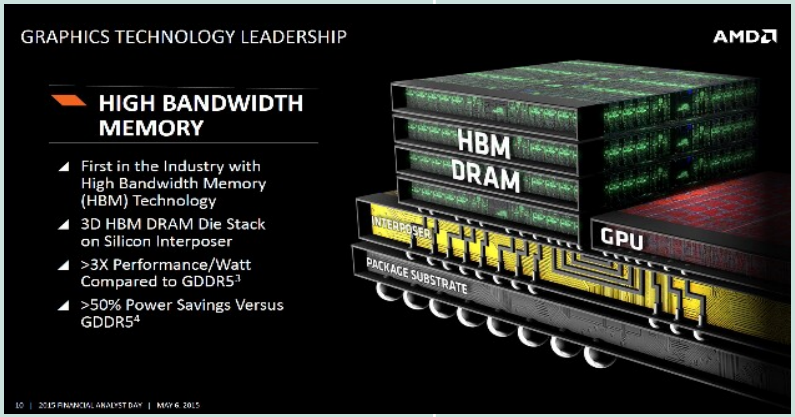
➔ Waferlevel Systemintegration using TSV

- Thinfilm technologies, Bumping
- Wafer thinning, Thin Wafer Handling
- Through Silicon Via (TSV) Formation
- High density metallization, redistribution
- Interposer, assembly and interconnection technologies









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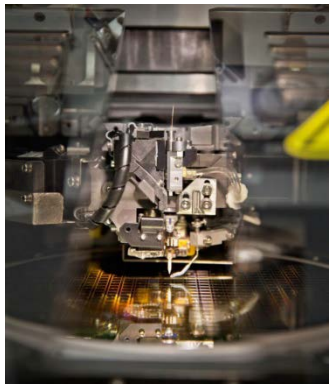
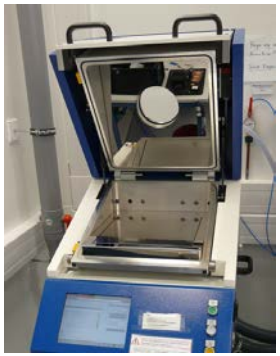
New Assembly Cleanroom



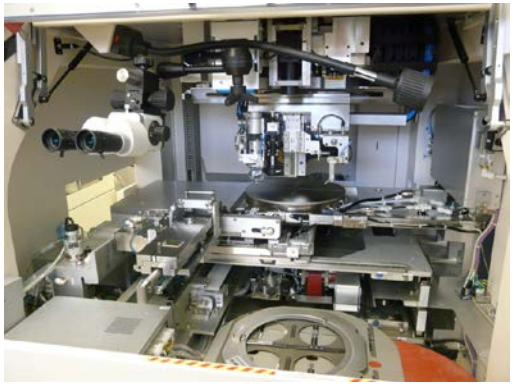
Wafer Stud Bumping
300 mm (K&S)

Surface Plasma
Protection
(ONTOS)



Batch Reflow Oven up to
300 mm (ATV, Budatec)

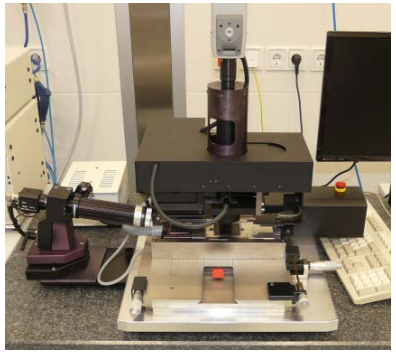
Low Pressure
Membrane Bonder
(ATV)



Automatic Die Bonder
300 mm
(BESI)

Automatic Flip Chip
Bonder 300 mm
(PANASONIC)

High Precision
Flip Chip Bonder
(SET)



Halfautomated Flip
Chip Bonder
(Finetech)

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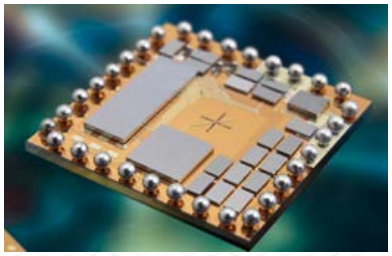
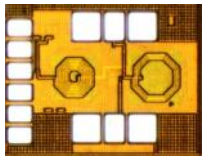
Waferlevel Systemintegration - Wireless Sensor Nodes

Features: Working range 50m, 12mm accuracy

Devices:

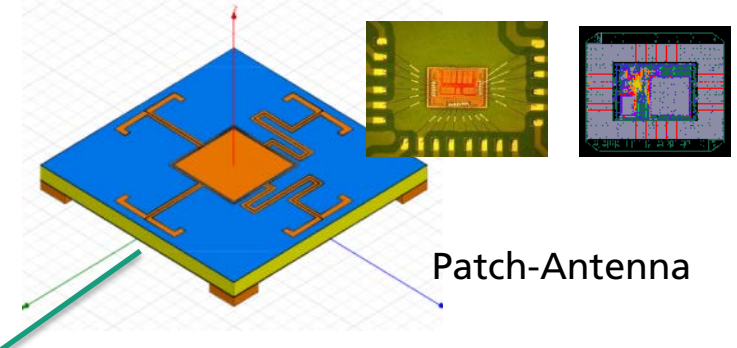
- FFT-Co-Processor, ADC
- Fractional-N-PLL
- LNA, PA, Mixer, VCO, Muliplexer





Package

- Thinfilm substrate
- Integrated patch antenna
- FC Device integration

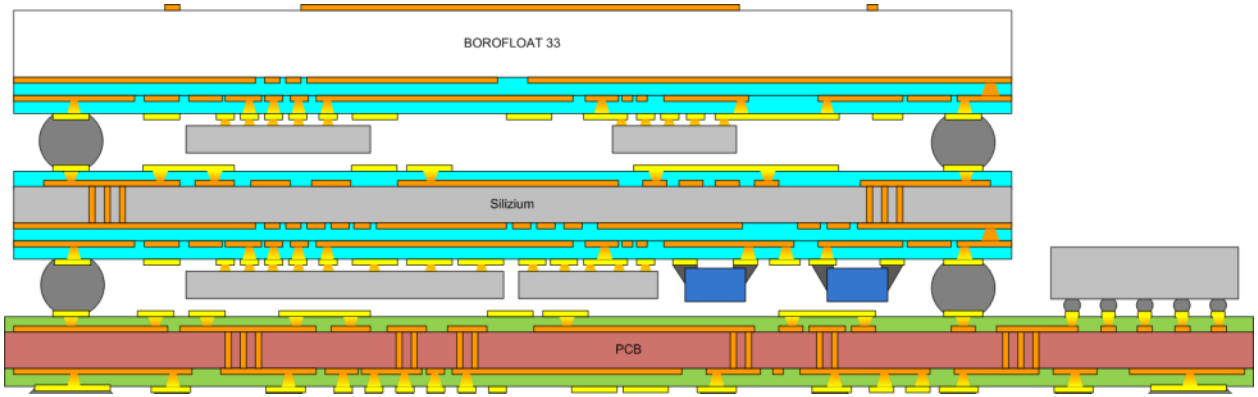


Patch-Antenna

RF – Substrate

Baseband-Substrate

Board (PCB)



TU Clausthal

Friedrich-Alexander-Universität Erlangen-Nürnberg

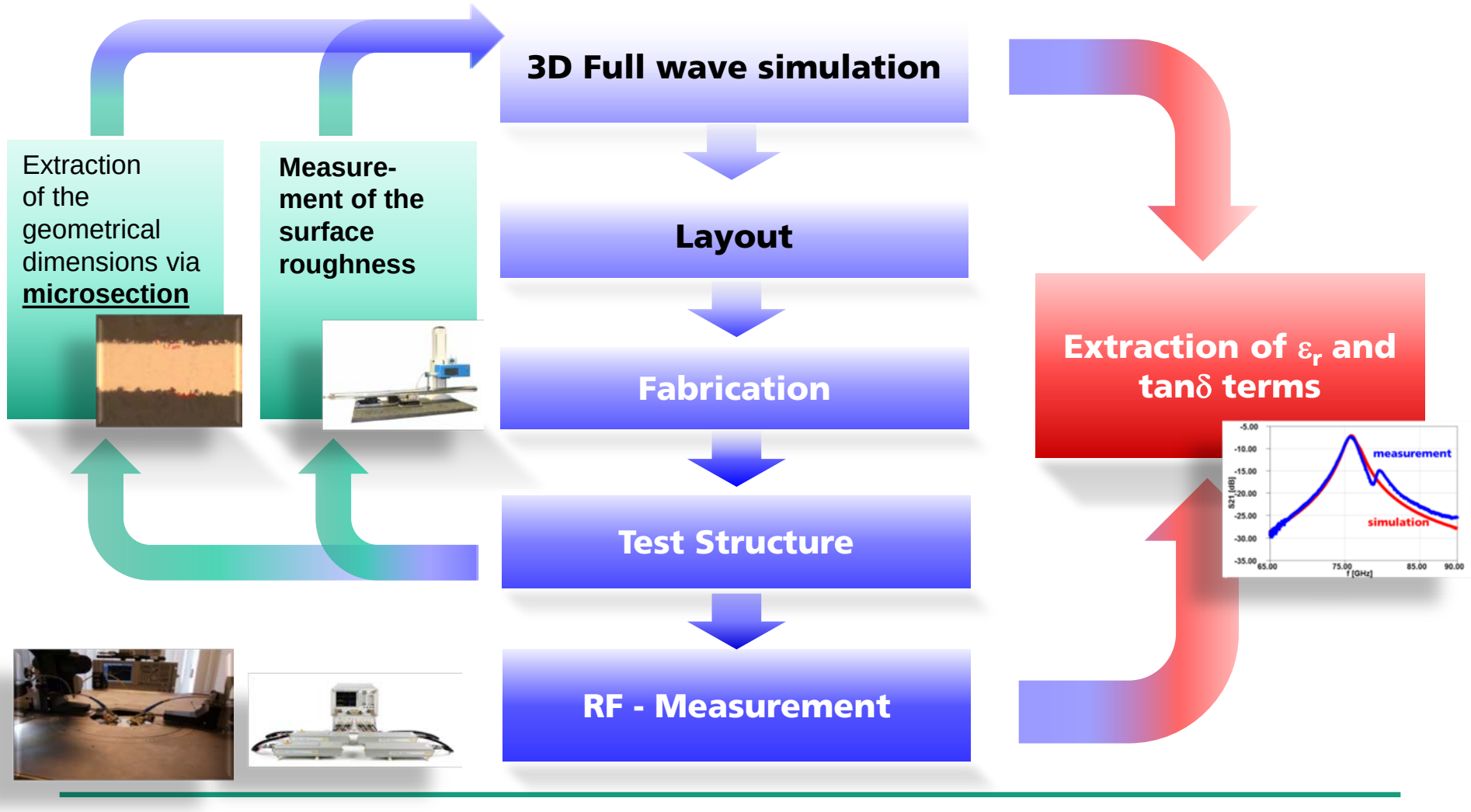
Leibniz Ferdinand-Braun-Institut

Bundesministerium für Bildung und Forschung

Fraunhofer IZM

Procedure for Extraction of Dielectric Parameters at >100 GHz

Department: RF & Smart Sensor Systems



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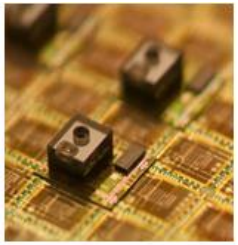
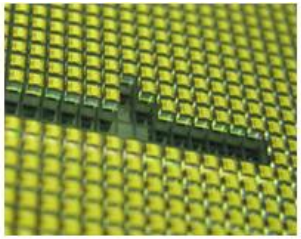
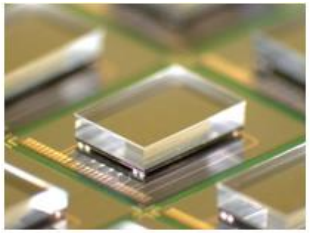
3D WL Integration (ICs + Sensors) @ Fraunhofer IZM



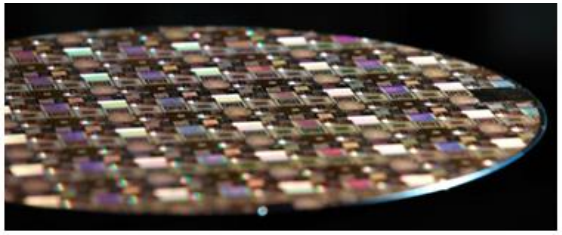
3D TPM
(ASIC+TX+MEMS)



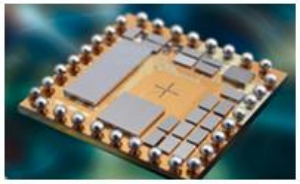
WL Camera



ASIC+Memory



IP –IP (G3)



Localization SiP

ARM Sensor

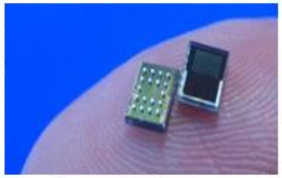
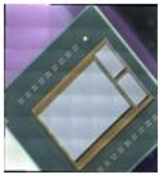
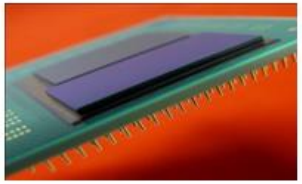


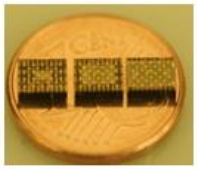
Image Sensor

MEMS

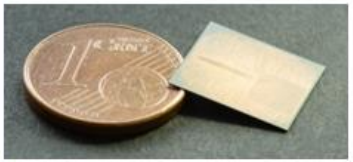




TSV Interposer (MPU+MEM)

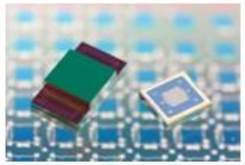


MEMS /ASIC

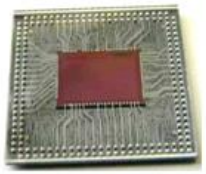


IP wide memory

TCI (Sensor+ASIC+TX)



MEMS



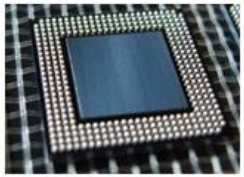
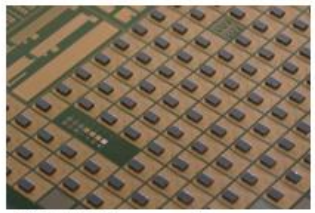
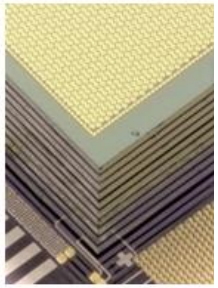


Image Sensor (Sensor+IP+SP)



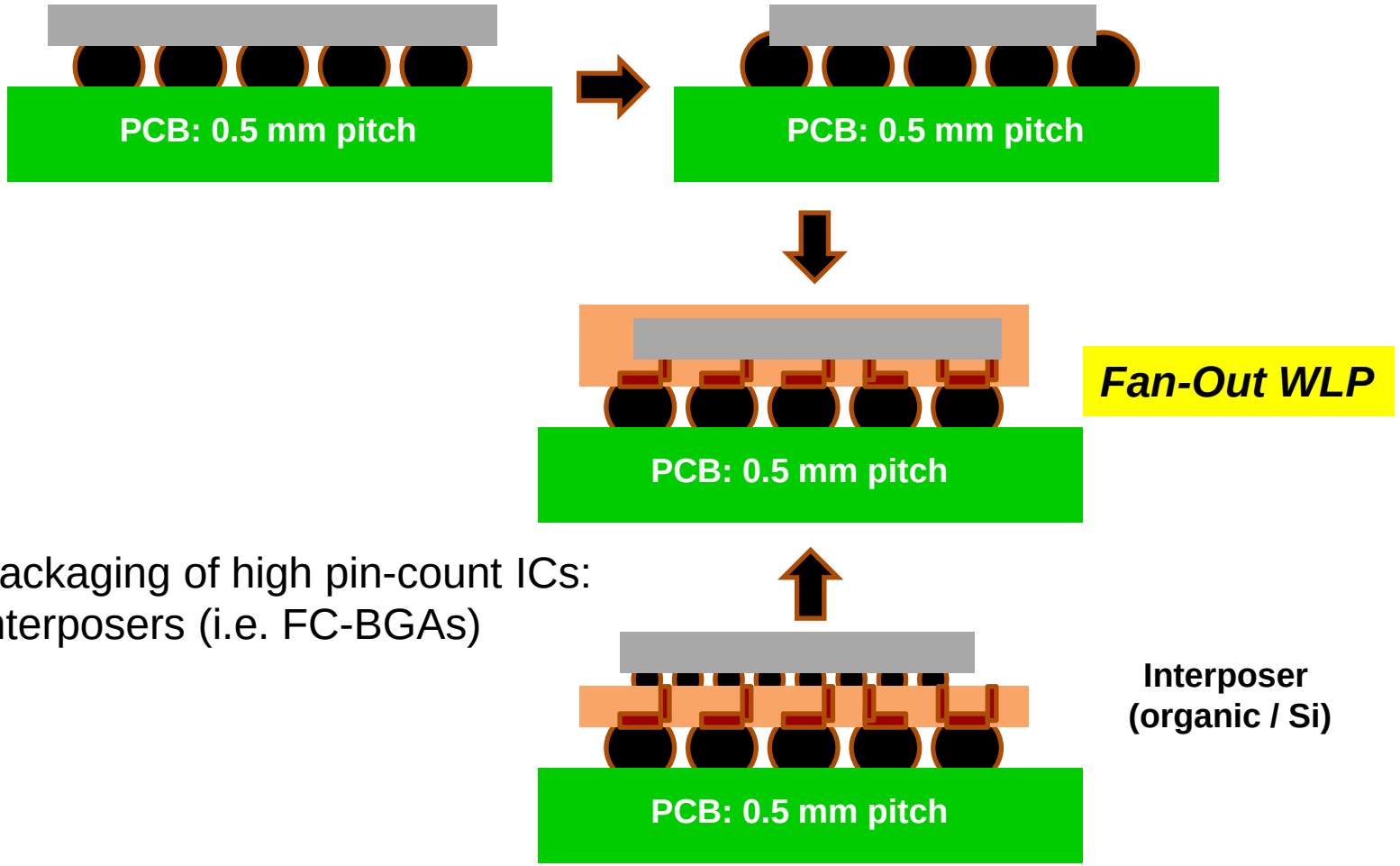
RF IP Transceiver



10x TSV stack

Future of WLP?

Fan-In WLP: Issue with miniaturization in Front-End (CMOS)

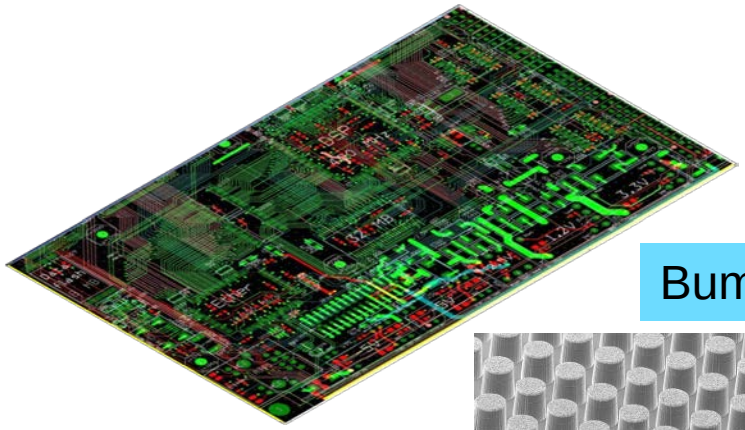


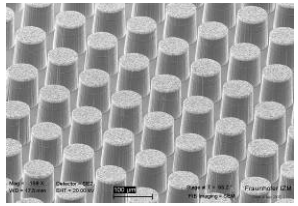
Packaging of high pin-count ICs:
Interposers (i.e. FC-BGAs)

PWB Design Rules ⟷ CMOS Design Rules

PWB (organic substrate)
Lowest Cost

CMOS (Si-based Wafers)
Highest Cost

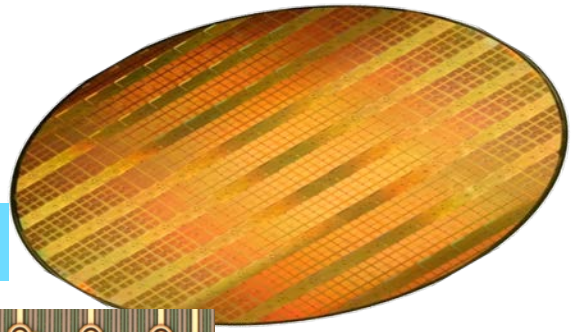


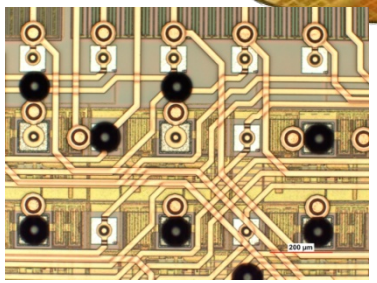


Bump

GAP

RDL/BEOL

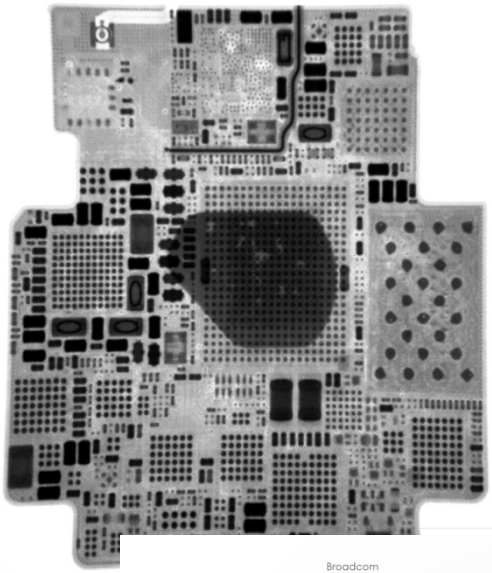




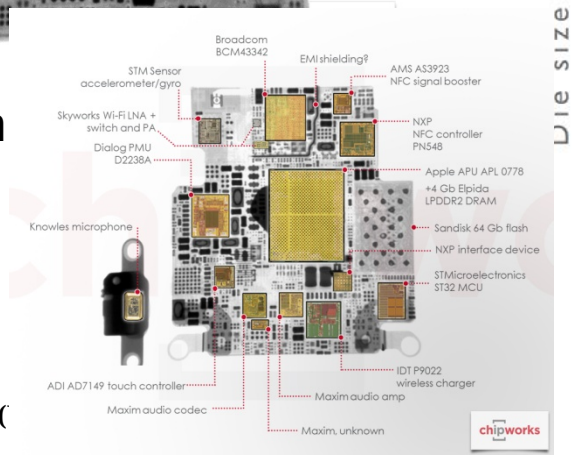
100 µm ← PCB Design Rules 50 µm …1 µm CMOS Design Rules → sub µm

Issue with WLP: Chip Shrinkage ➔ Solution ➔ Fan-Out

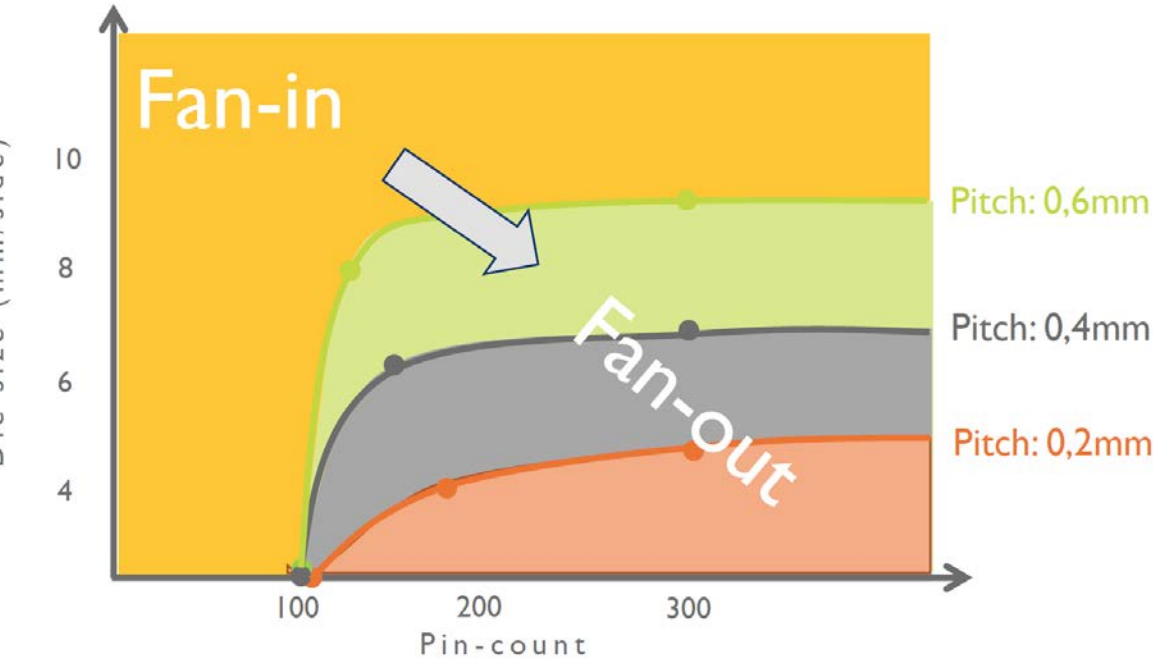
For SMD-Assembly 0.5/0.4 mm ball pitch is required
(yield and speed of assembly)



iWatch



Solution: Extension of Chip Surface by FO-WLP



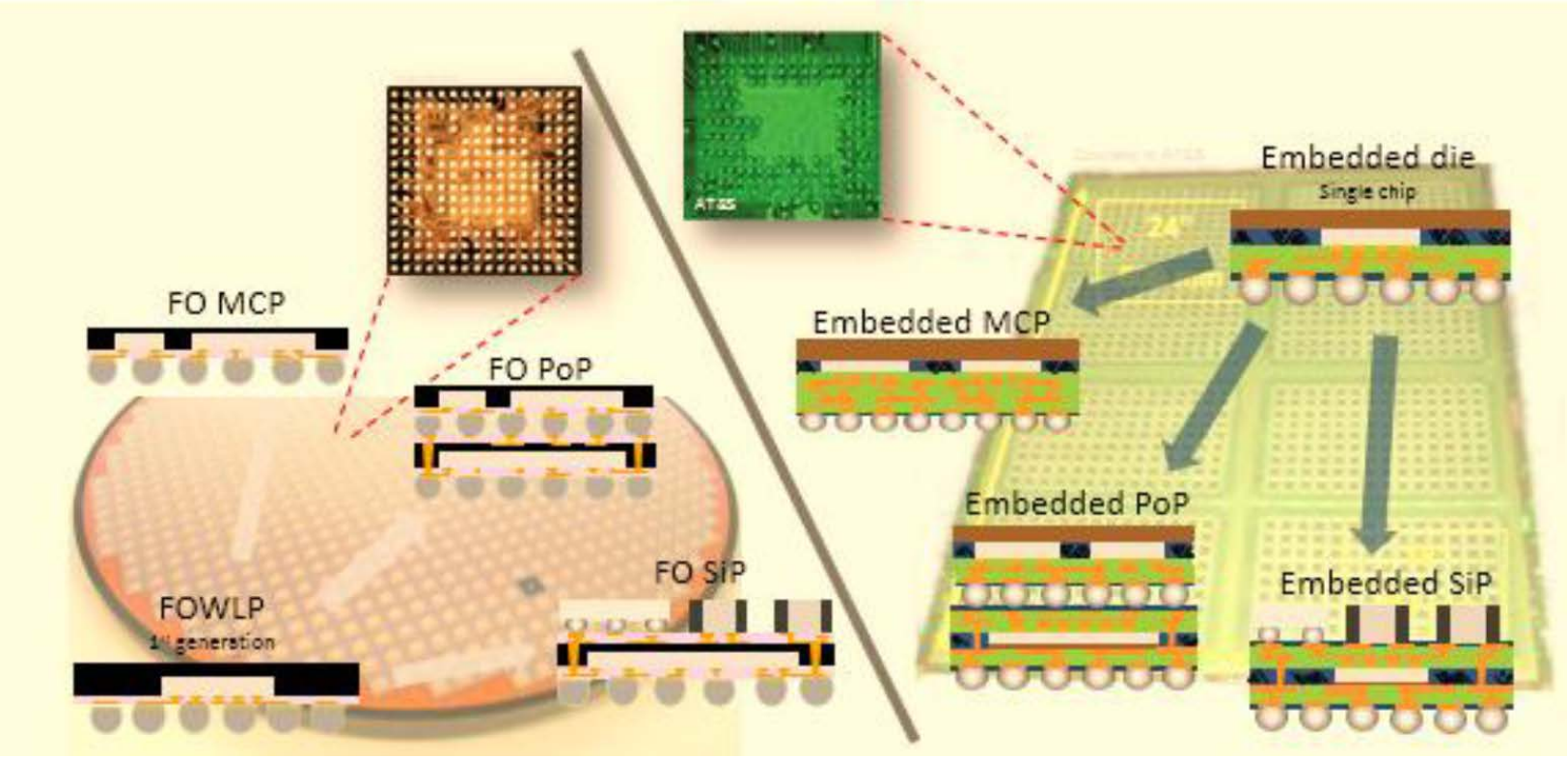
Fraunhofer IZM

➔ Chip Embedding (Chip into Substrate)

Multi-Chip Package and 3D is possible

Embedding die technology:

- ➔ Embedding into PWB (embedded die)
- ➔ Reconfigured molded wafer. FOWLP (Fan-Out Wafer Level Packaging)

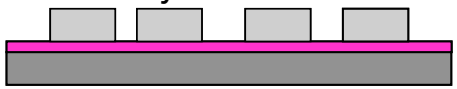


FOWLP/FOPLP Process Flow Options

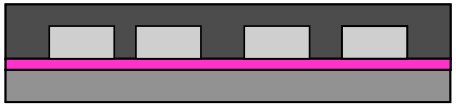
Mold first

Apply thermal release tape on carrier

Die assembly on carrier

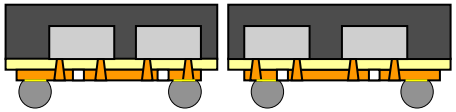


Wafer/panel overmolding



Carrier release

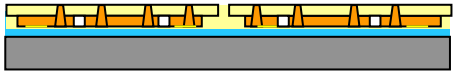
RDL (e.g. thin film, PCB based, …), balling, singulation



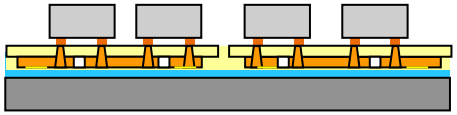
RDL first

Apply release layer on carrier

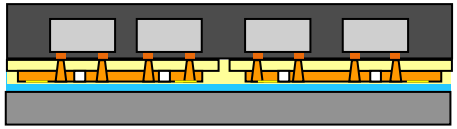
RDL (e.g. thin film, PCB based, …)



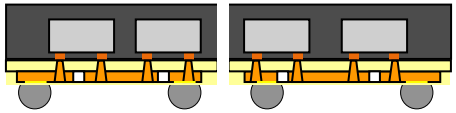
Die assembly on carrier

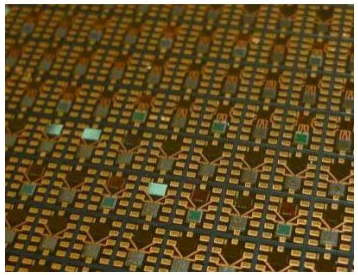


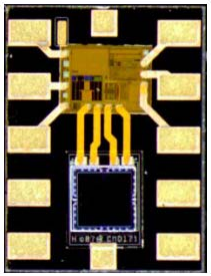
Wafer/panel overmolding



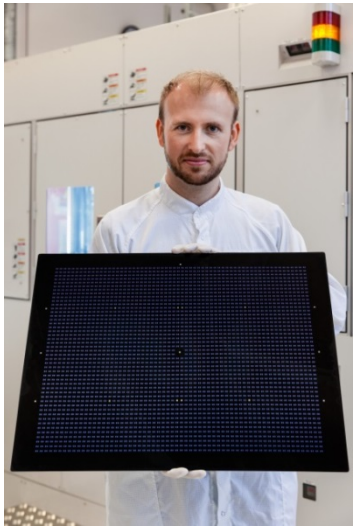
Carrier release, balling, singulation







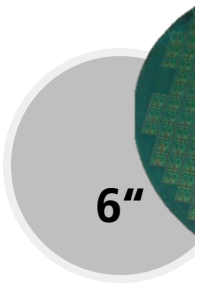
Pressure Sensor-ASIC Package



Fraunhofer IZM

From Wafer to Panel Level Packaging

- Based o
  equipme
- Tightest
  line/spa
- Currentl



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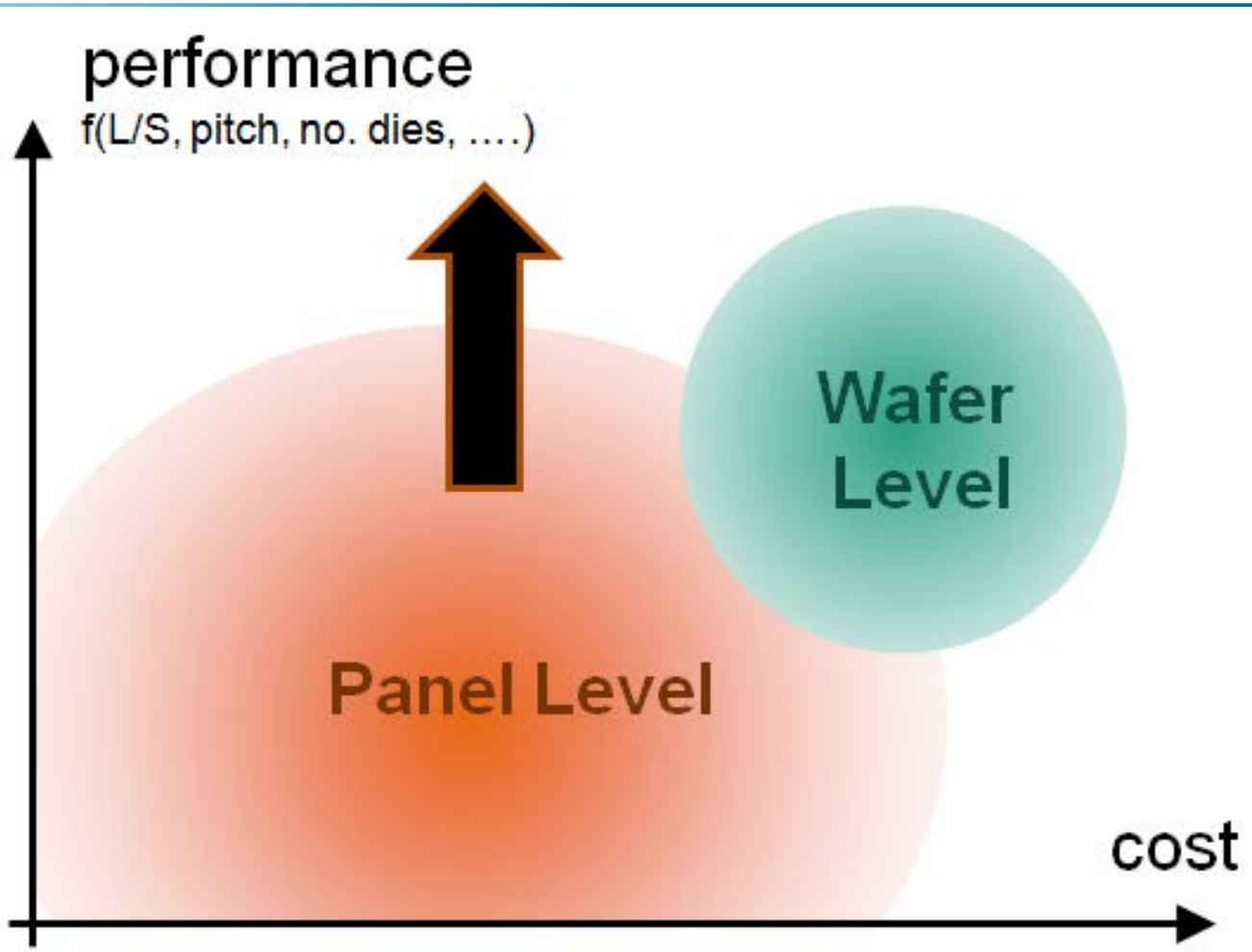


cturing

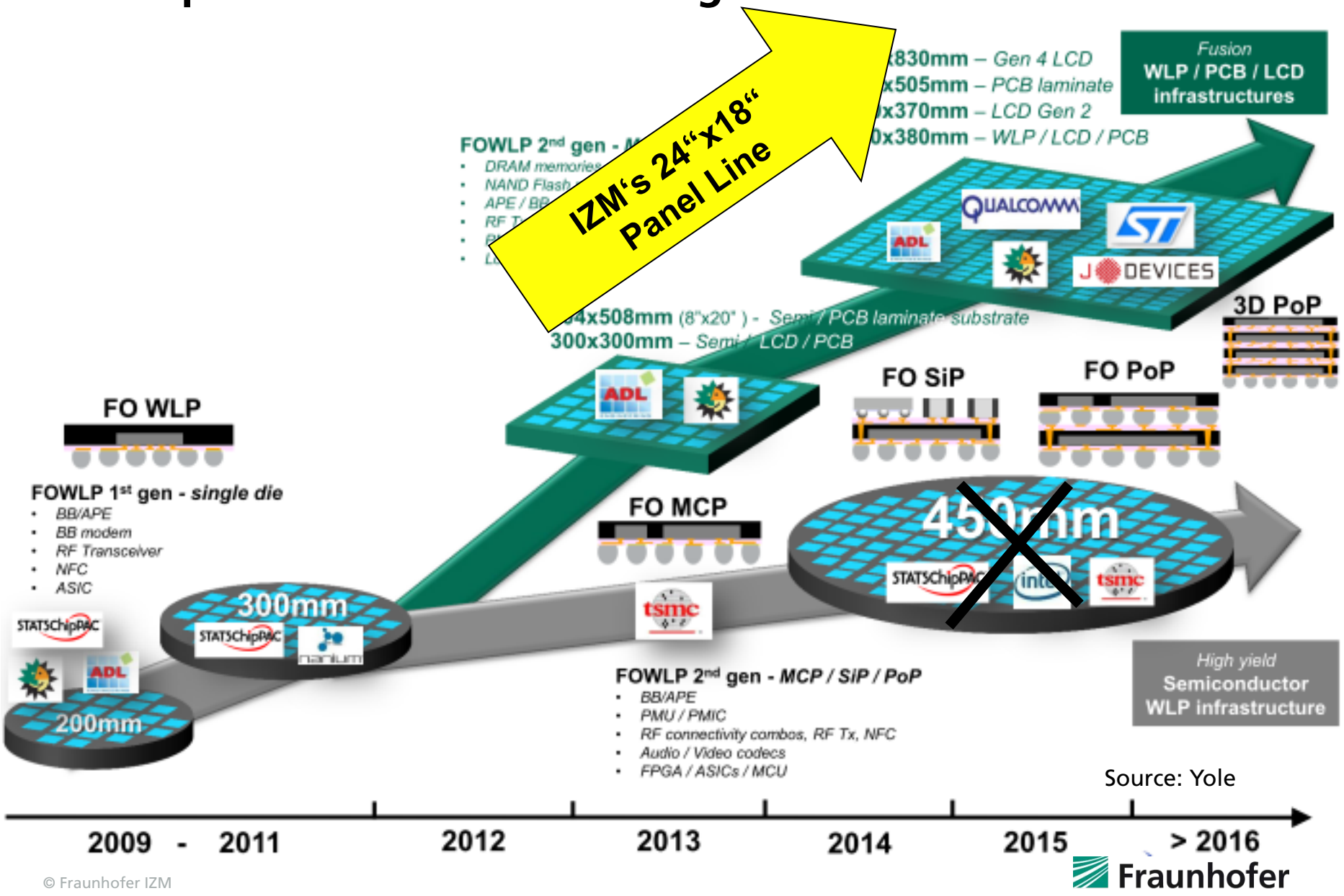
n by

e
ne/space

rd

x18“

Roadmap Panel Level Embedding



Fraunhofer IZM

IZM Panel Level Embedding Line
from Wafer Scale to Panel Scale 610 x 456 mm²/24”x18”

Placement

Datacon/Siplace

Accuracy

Inspection

Molding

Panel Molding

Lamination

Laminator

Laser Drilling

Laser Equipment

Via Drilling

mech. drilling

Seed Layer

Sputter

Cu Plating

Automatic plating line

Imaging

LDI

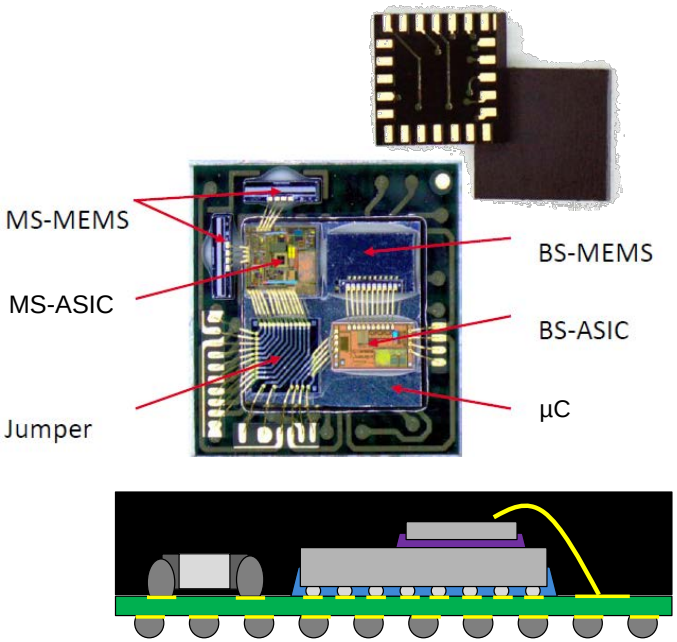
Etching

Wet Etching

Fraunhofer IZM

MST SmartSense - Intelligent 3D MEMS Compass

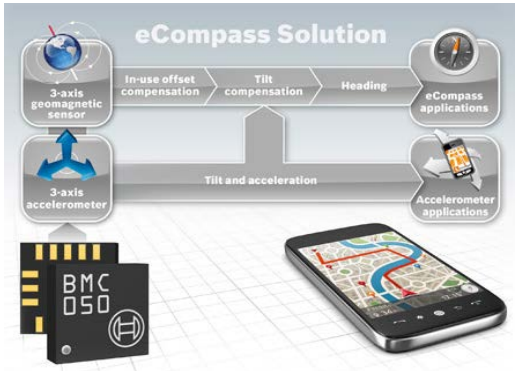
Technology Demonstrator

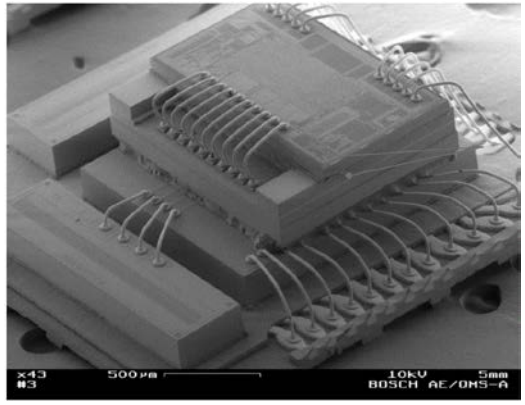


Heterogeneous Integration

- BGA Multi-Sensor Package
- Evaluation of Material Combinations
- Reliability Investigations

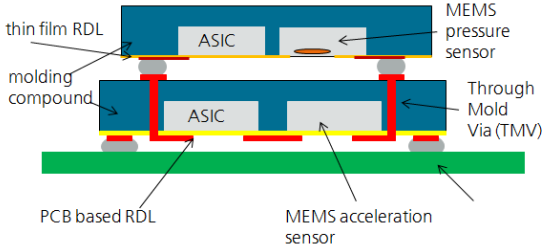
Commercial Product

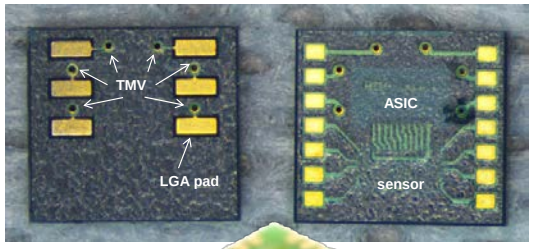


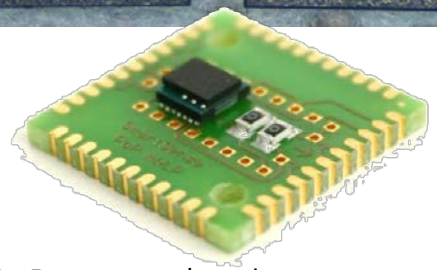


- Chip on Board technology
- Transfer molded LGA housing

Advanced Technology



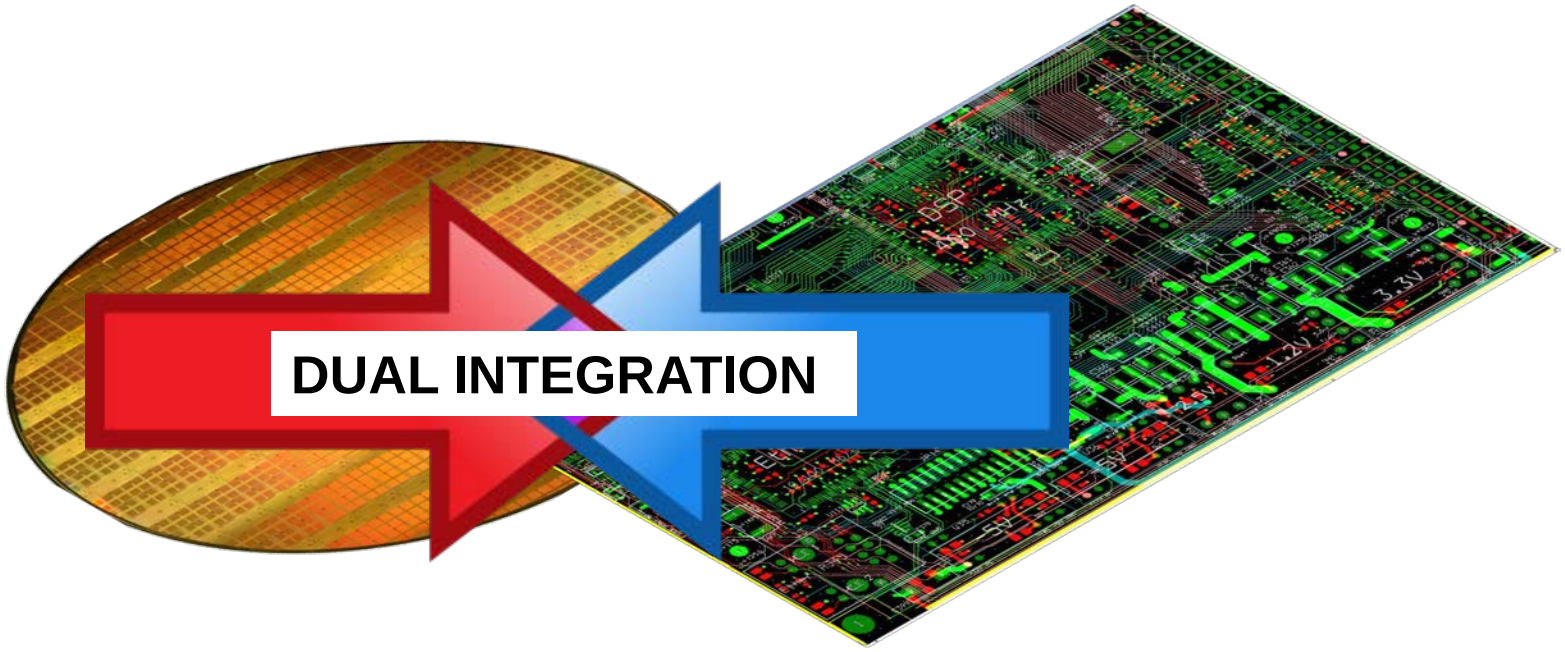




- PoP approach using embedding as a basis
- Thin film & PCB based RDL
- Product well within specs!

Fraunhofer IZM

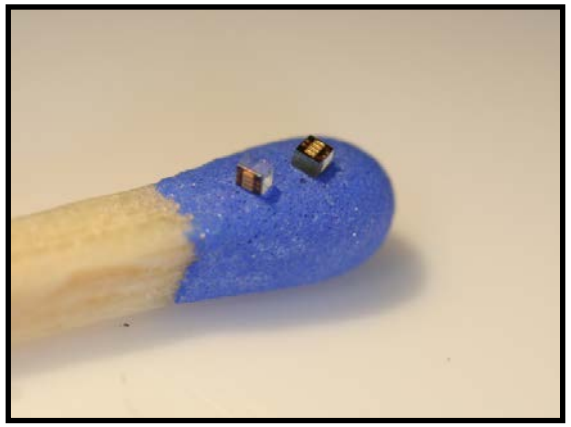
Summary

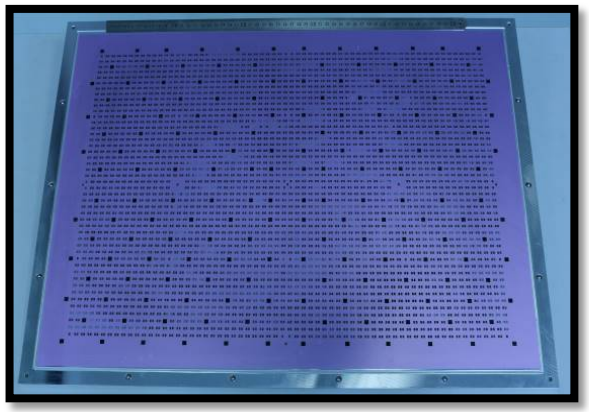


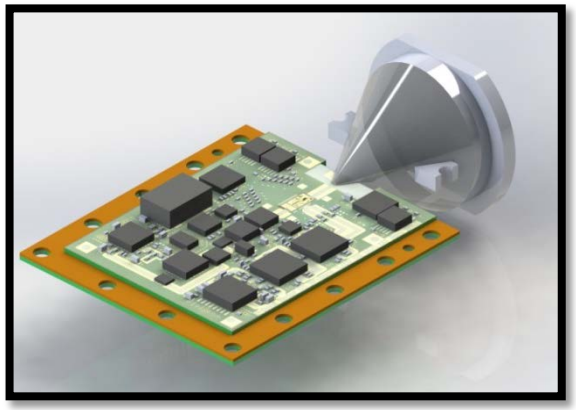
Miniaturization

Cost

Electrical performance



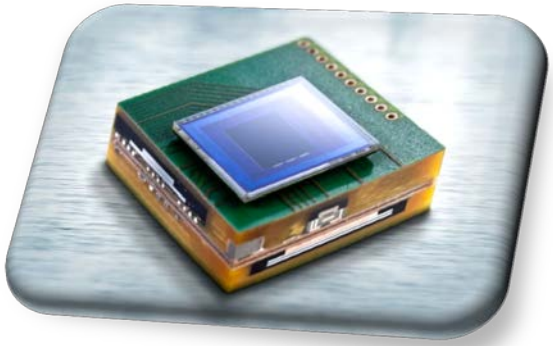




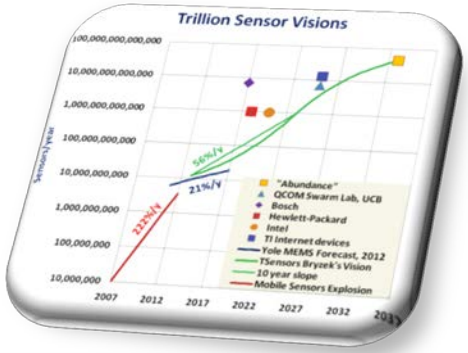
Automotive, Medical
Industry 4.0

Internet of Things
Consumer

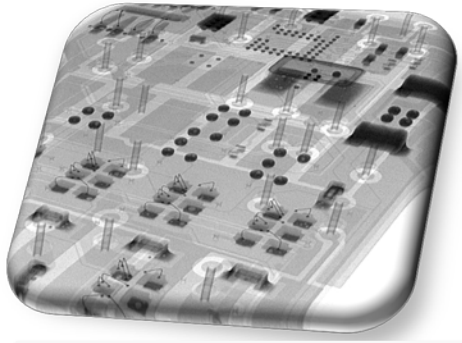
RF-Modules
Mobile Wireless



Camera with image processing



Trillion Sensor Vision



X-ray of embedded System

Fraunhofer
IZM