ERÖFFNUNG DES INNOVATIONSZENTRUMS ADAPTSYS

Höchstintegrierte Leistungselektronik mit hoher Zuverlässigkeit

Prof. Eckart Hoene
Leistungselektronik

Fraunhofer IZM

Agenda

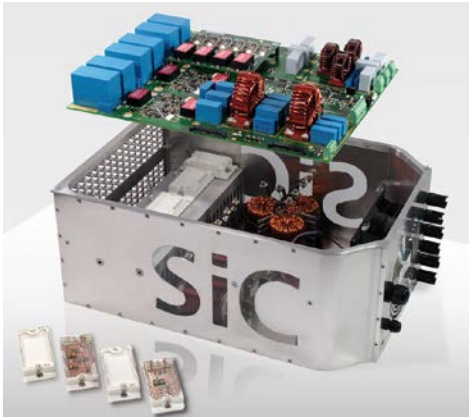
- Motivation
- Schlüsselinnovationen in den aktuellen Demonstratoren
- Heterogene Integration als nächste Innovation
- Aussichtsreiche Technologien
- Resumé

Motivation

Leistungselektronik kann Energie mit unübertroffenem Wirkungsgrad in die benötigte Form bringen, damit

- ist sie ein Schlüsselelement für die dezentrale Energieerzeugung und die Reduktion des Energieverbrauchs

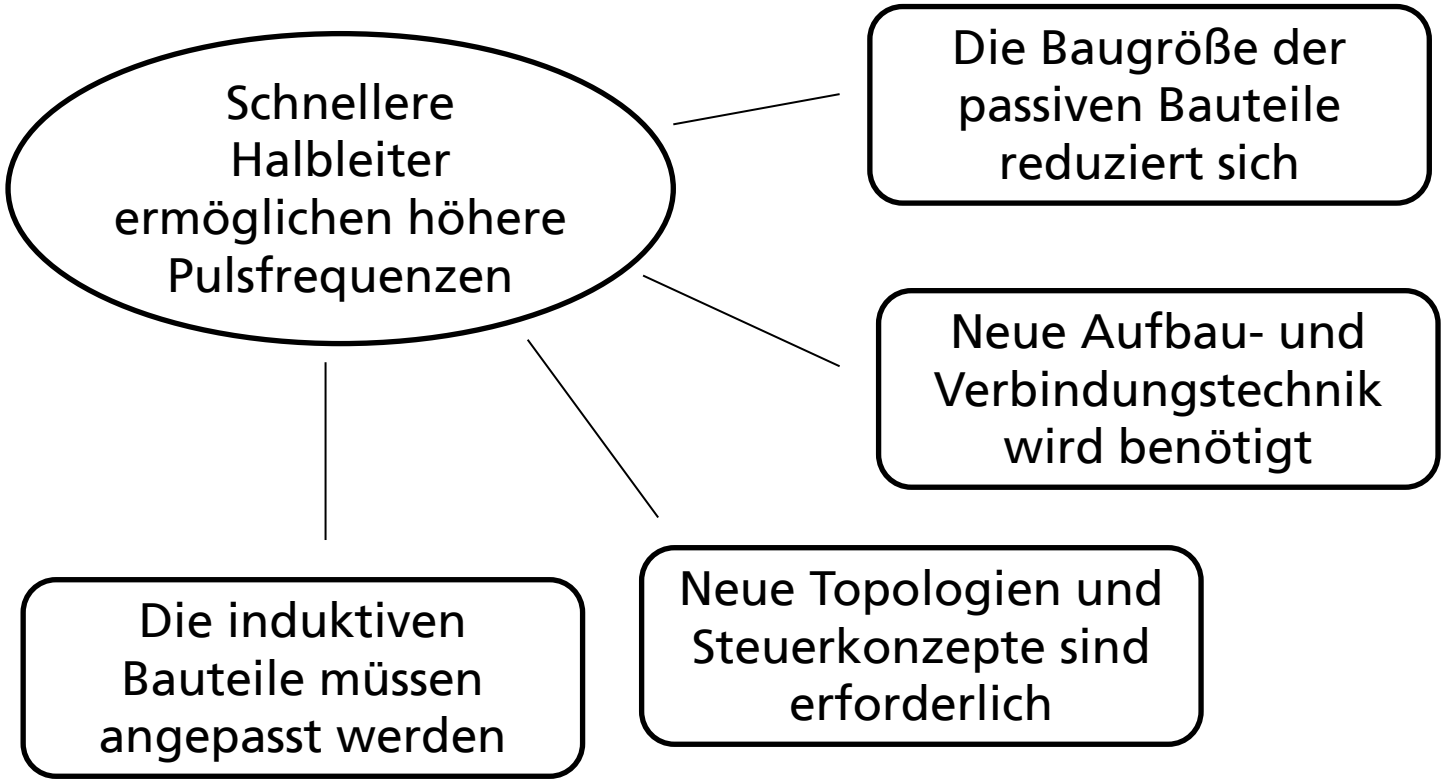
Ziel muss sein, den Aufwand für ihre Herstellung so weit wie möglich zu reduzieren, um den massenhaften Einsatz zu forcieren



IZM Gen.1 (2012)
SiC JFets, 48 kHz pulse frequency
18l - 18,4 kg (15kW)
Conventional Packaging

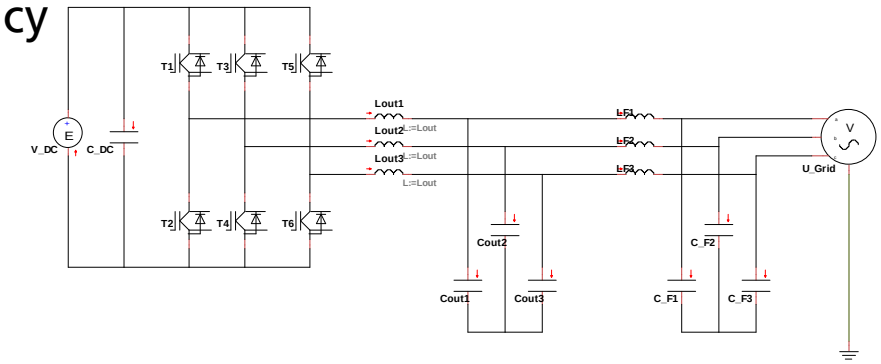
IZM Gen.2 (2015)
SiC MOSFets, 250 kHz pulse frequency
2,4l - 4 kg (15kW)
Embedded Power modules

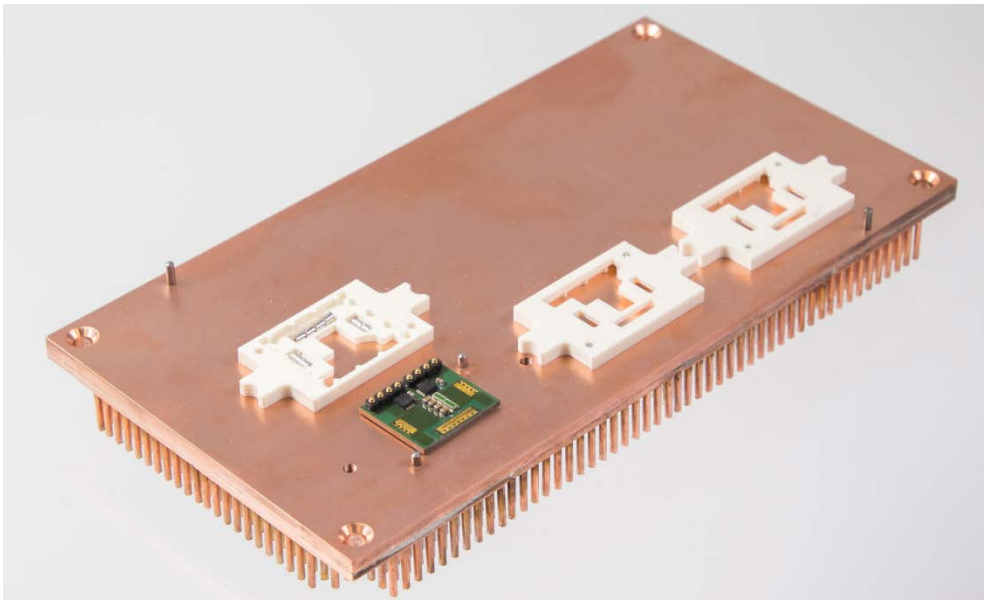
Wie konnte so ein Fortschritt erreicht werden?



Schlüsselinnovationen in Gen 2

- Simple topology, high pulse frequency
- Semiconductor packaging
- Operation scheme
- Inductor design
- Filter design



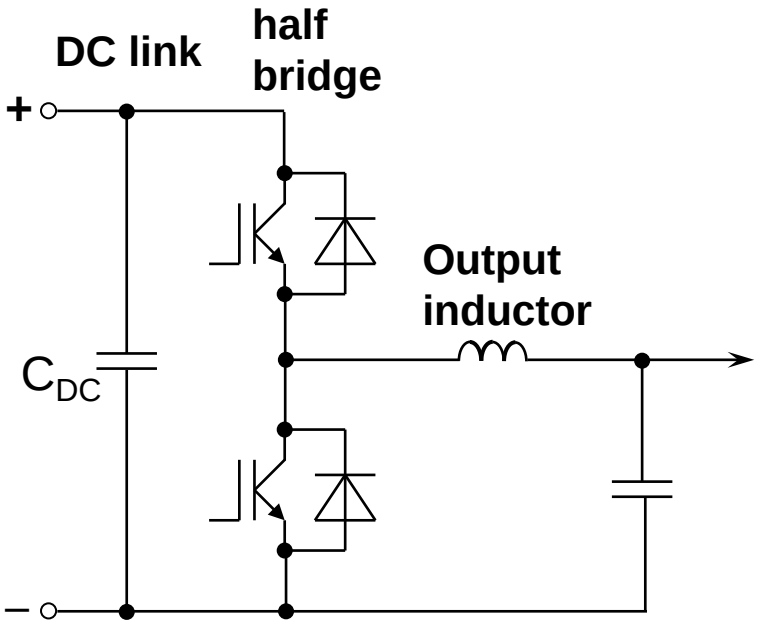


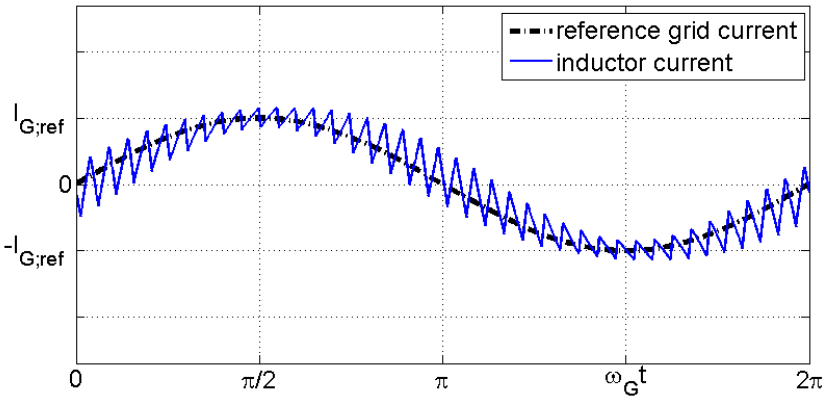
Fraunhofer IZM

Schlüsselinnovationen in Gen 2

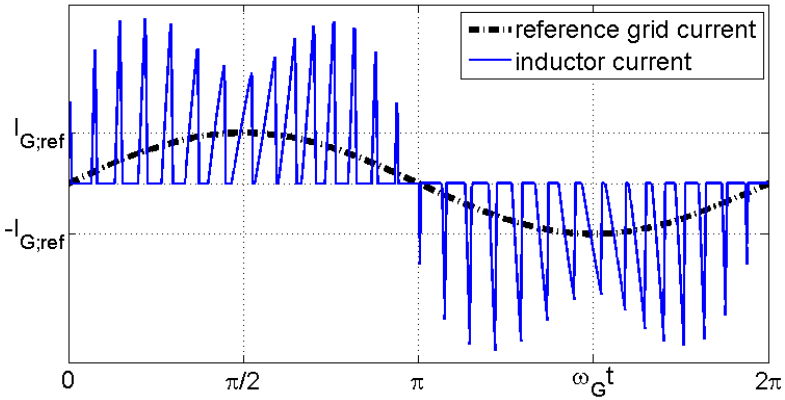
- Simple topology and high pulse frequency for low component number count
- Triangular current mode (TCM) for small output inductor and recovery of energy stored in semiconductor capacitance
- Variable pulse frequency to allow ZVS and reduce measured interference level
- Encapsulated EMI Semiconductor Packaging (EESP) to reduce EMI filter effort
- Revolutionary inductor design for output inductor
- High effort driver to accelerate SiC-Mosfets

Schlüsselinnovationen in Gen 2





Discontinuous current mode DCM

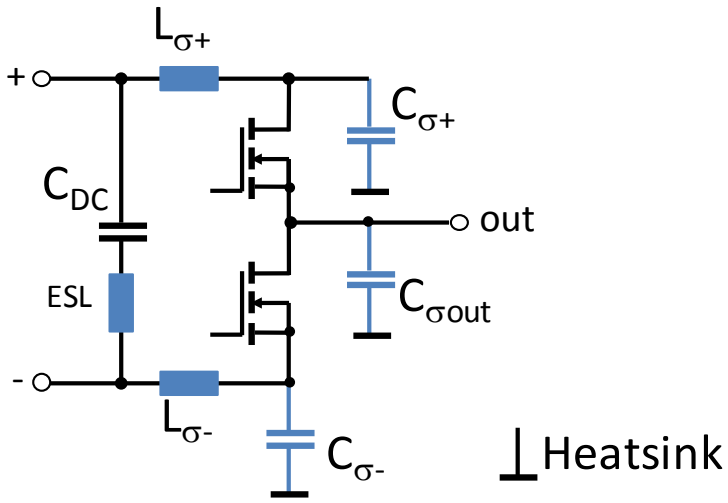


- Benefits of DCM in comparison with CCM
  - Inductance value is lower by a factor of app. 100 → volume essentially lower
  - No semiconductor turn on losses

Fraunhofer IZM

Schlüsselinnovationen in Gen 2

The parasitics coming from the switching cell

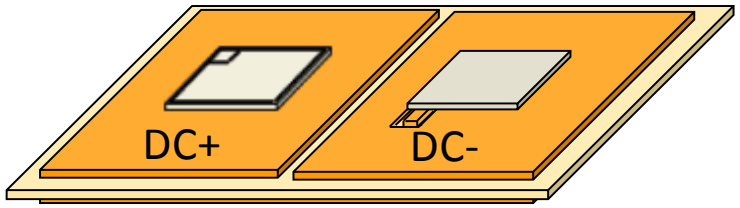


Which parameters are critical in the module?

- $L_{\sigma+}$, $L_{\sigma+}$ and ESL form the DC link inductance
- $C_{\sigma out}$ is reloaded with every switching event and originates a current in the heat sink -> EMC problems
- If C_{σ} or L_{σ} are unbalanced, a current into the heat sink is generated -> EMC problems

Schlüsselinnovationen in Gen 2

The Next Generation Package

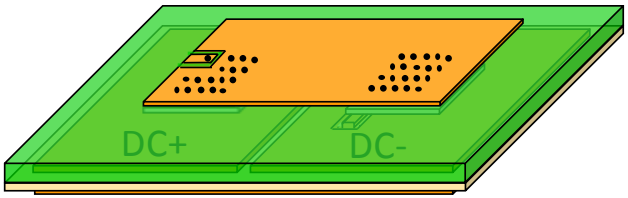


Solution:

- A ceramic substrate for safety insulation
- High and low side switch to complete the switching cell in the package
- DC+ and DC- lands with same size and geometry for balanced parasitics
- Low side chip flipped to avoid tracks carrying out potential

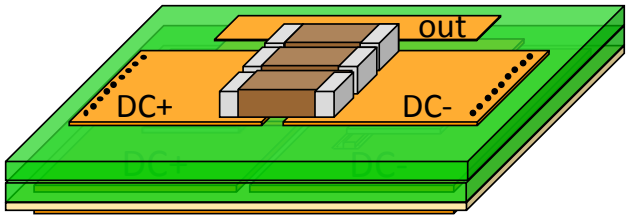
Schlüsselinnovationen in Gen 2

The Next Generation Package



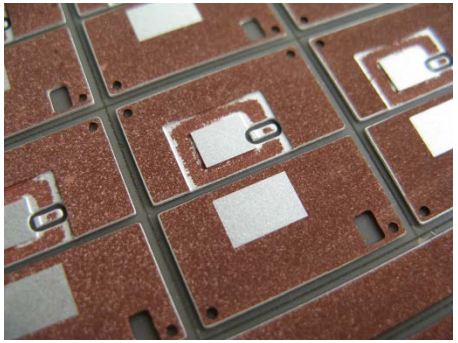
Next production steps:

- Embedding the chips in a PCB process and structuring the layer



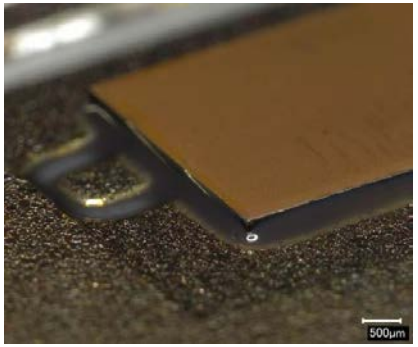
- Surface layer with primary DC link capacitors and optional driver components

Schlüsselinnovationen in Gen 2

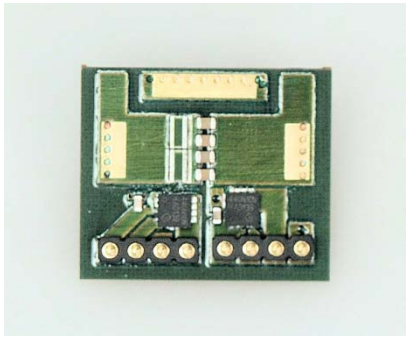


Silverpads on DCB

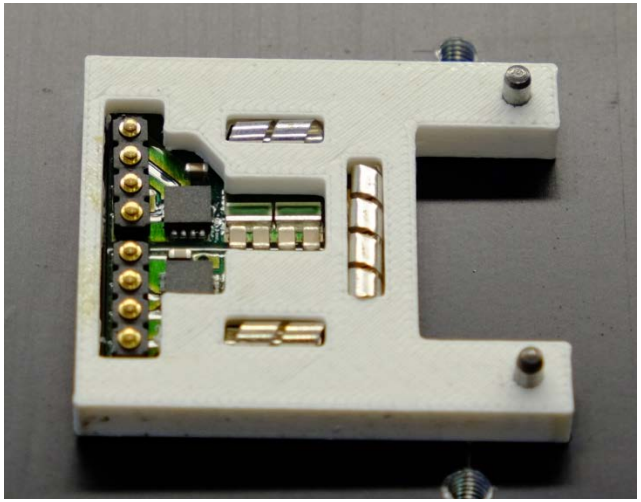
sintered chips



underfilled flip chip



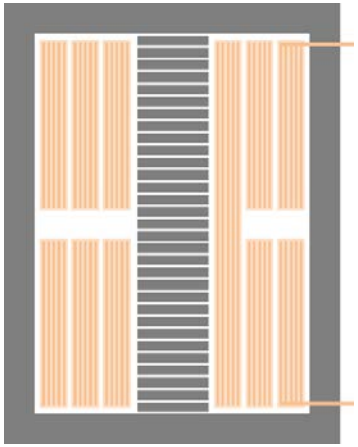
final module

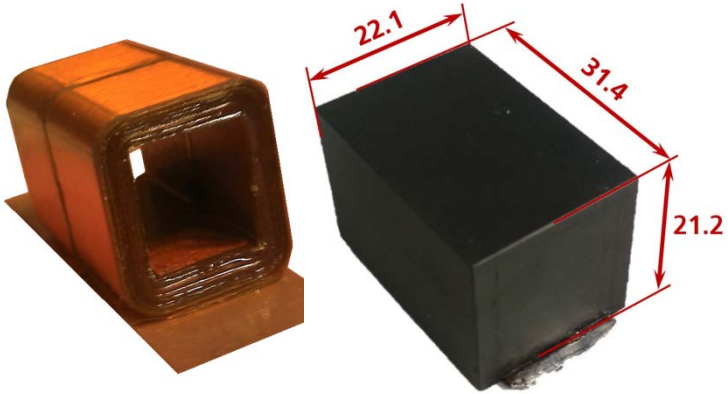


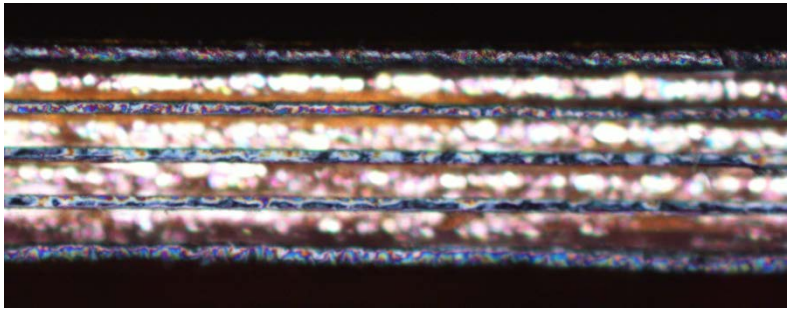
Module including plastic frame and springs

Schlüsselinnovationen in Gen 2

Completely altered design of inductors for high ripple+high frequency:
- high copper fill factor
- Skin&Proximity effect cancellation







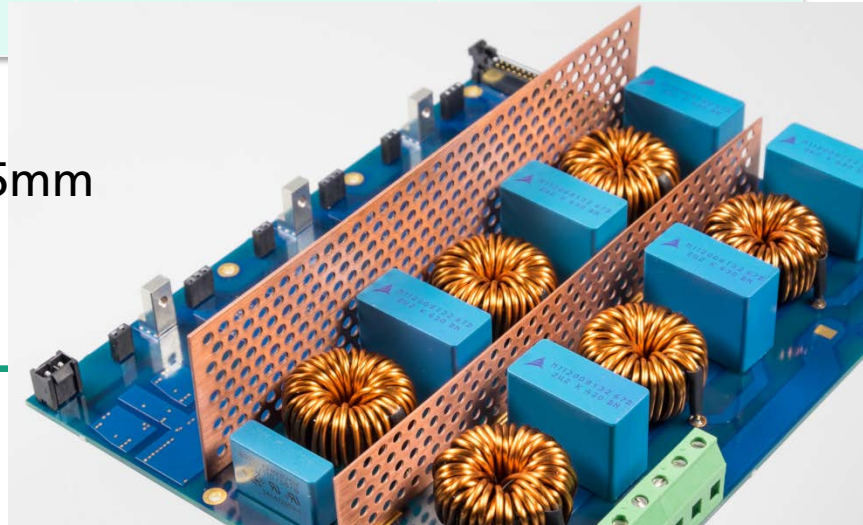
Foil stack with 22µm copper and 10µm insulation

Schlüsselinnovationen in Gen 2

- New EMI filtering concept

	State of the art	SOlar	VFS
Switching frequency	16kHz	48kHz	250kHz
Number of voltage levels	3	3	2
First frequency that has to be filtered f_1	160kHz	192kHz	250kHz
Limit value	55.5dBµV	54.0dBµV	51.8dBµV
Noise voltage @ U_{DC}=650V and f_1	143.3dBµV	151.3dBµV	169.3dBµV
Required filter attenuation @ f_1	87.8dB	97.3dB	117.5dB

- 2 DM filter stages required
- Filter dimensions l=107mm, b=98mm, h=35mm

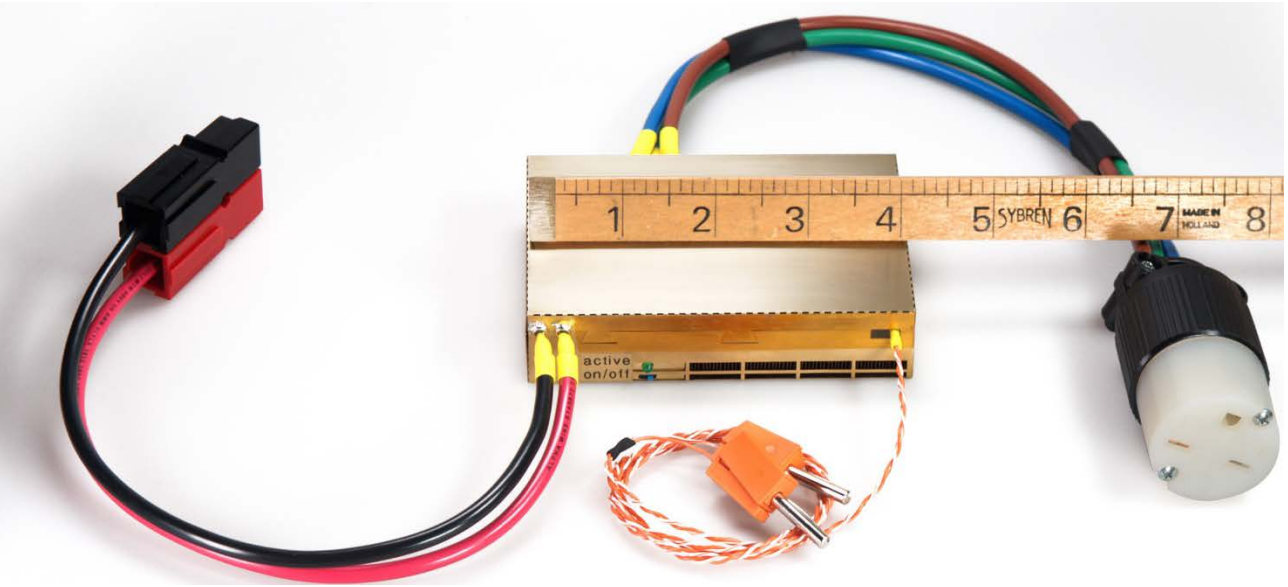


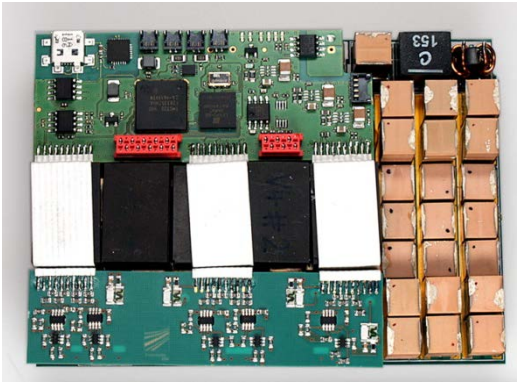
Aktuelle Generation 3

Fraunhofer IZM and ETH joined

LITTLE BOX CHALLENGE by Google

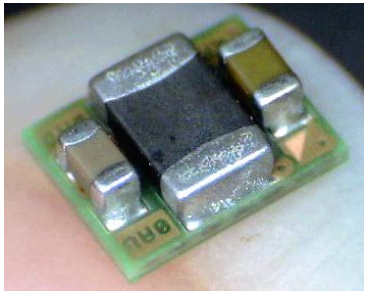
IZM Gen.3 (10/2015)
>300kHz
0,23l (2kW)
Innovation in topology, packaging, passive components, control



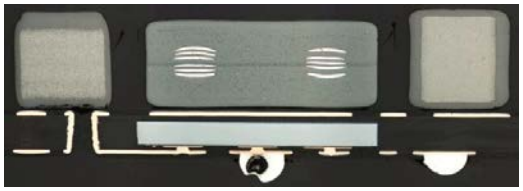


Heterogeneous Integration as next step

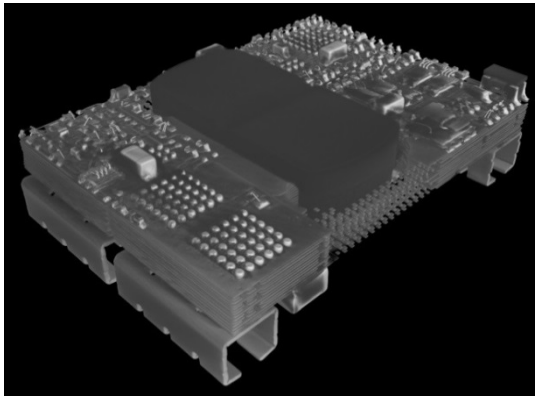
Two examples giving an idea on future development



Texas Instruments



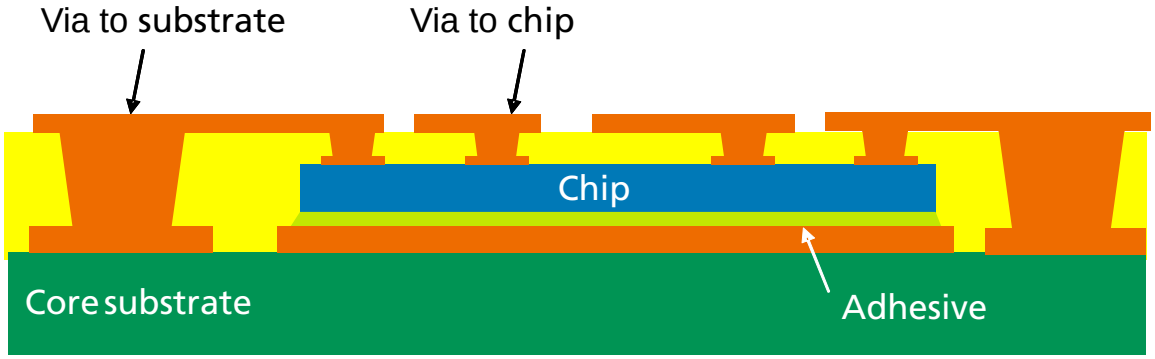
PCB with embedded semiconductors and SMD passives

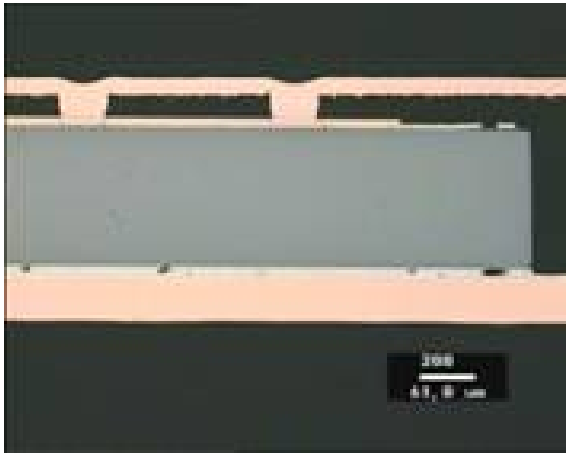


Multilayer PCB including coil windings, overmolded

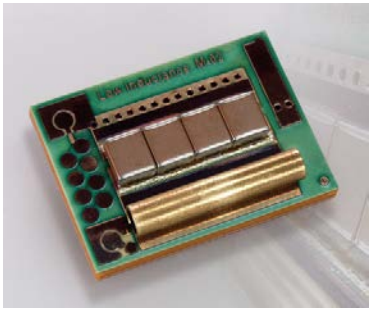
Heterogeneous Integration as next step

Embedding technologies

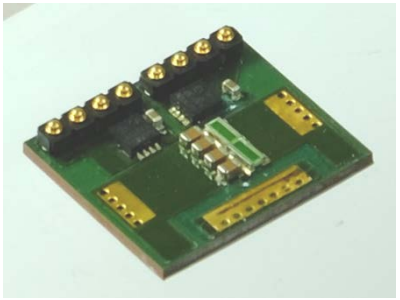




Examples for power modules in embedding on ceramic technology by IZM



1200V, 30A, world record in DC link: <1nH

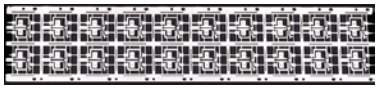


Heterogeneous Integration as next step

What is the benefit of embedding?

- Space saving on the PCB
- More freedom to design the electromagnetic parasitics beneficially
- Big production batches

Manufacturing on leadframes



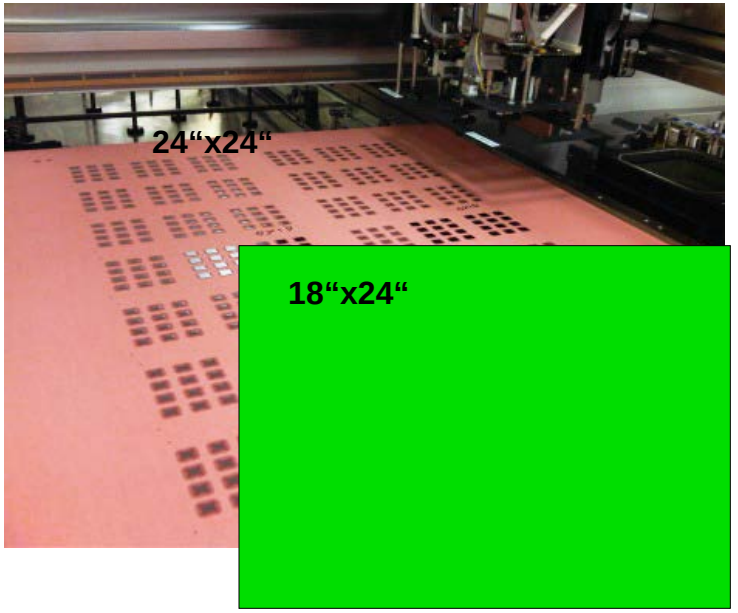
8“

~ 155 cm²

- **dominating technology**
- many process options
- cost optimised

➔ **OSAT**

Chip embedding in substrates



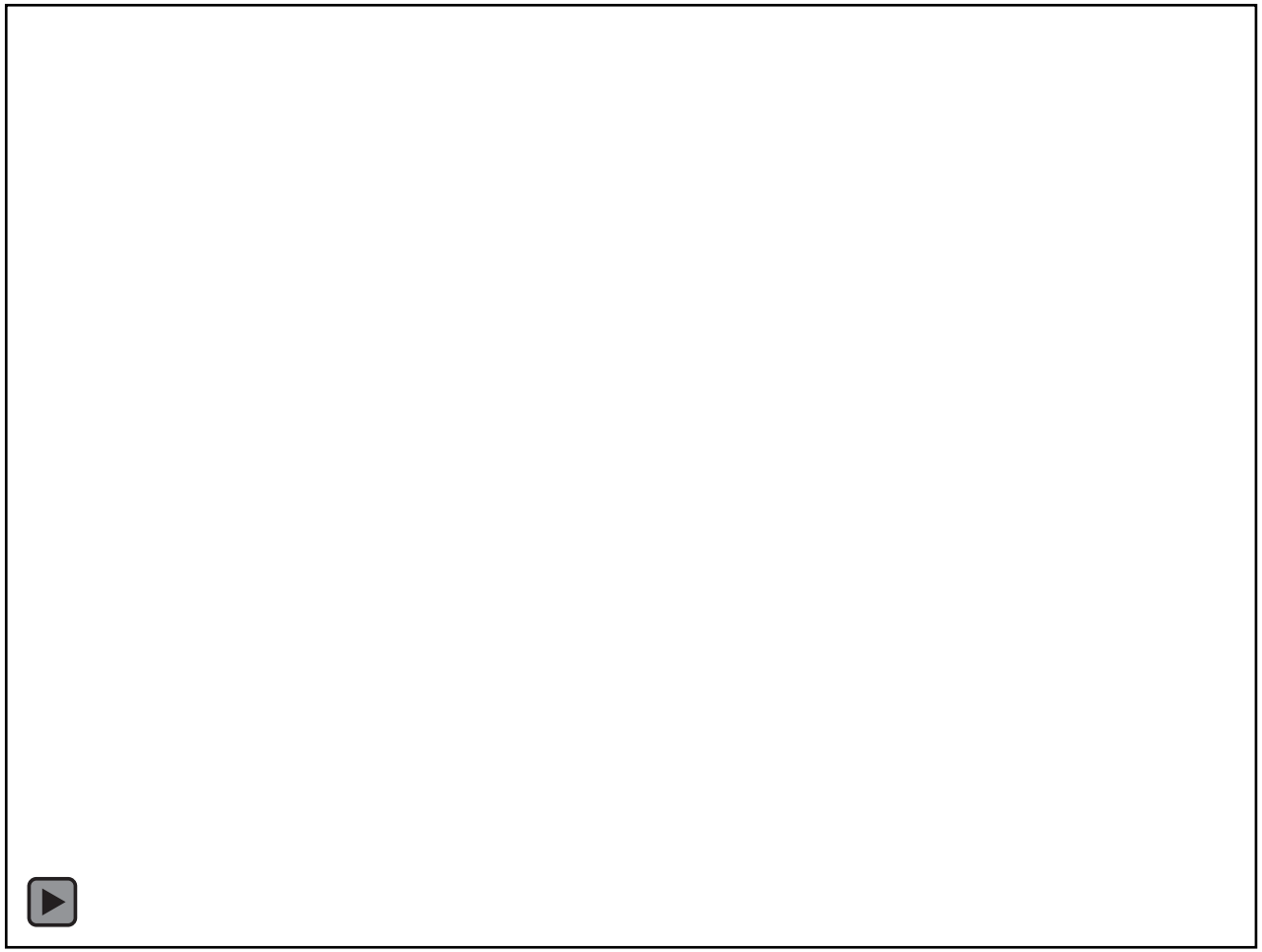
~ 2790 cm²

- **PCB technology**
- begin of production
- today low I/O chips
- intrinsic 3D and power capability

➔ **PCB manufacturers**

Heterogeneous Integration as next step

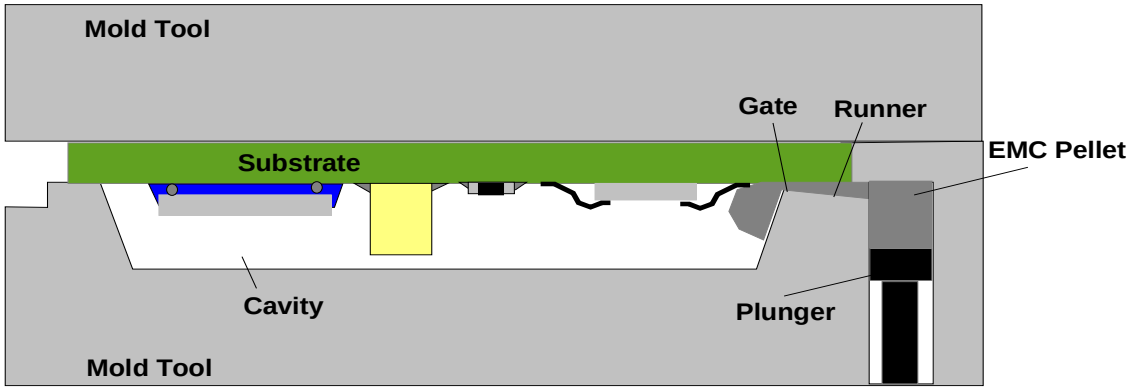
PSiP: Power System in package

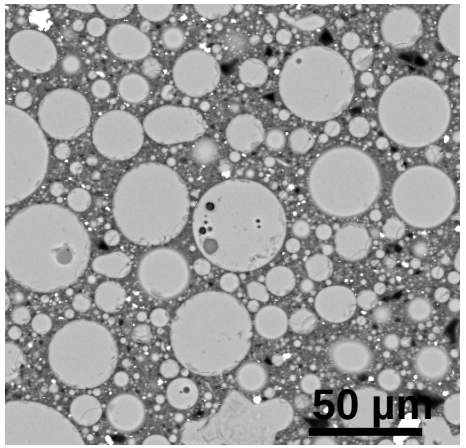


- Power ratings up to 1.8kW in 8 cm³
- Multi layer PCB also used for coils
- SMD or bare die assembly
- Transfer Mold encapsulation for thermal and handling reasons

Heterogeneous Integration as next step

Transfer Mold Technology

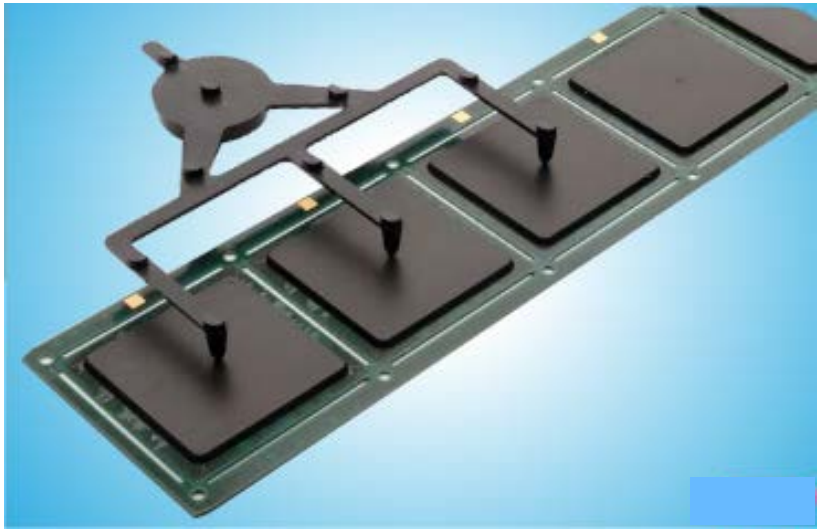




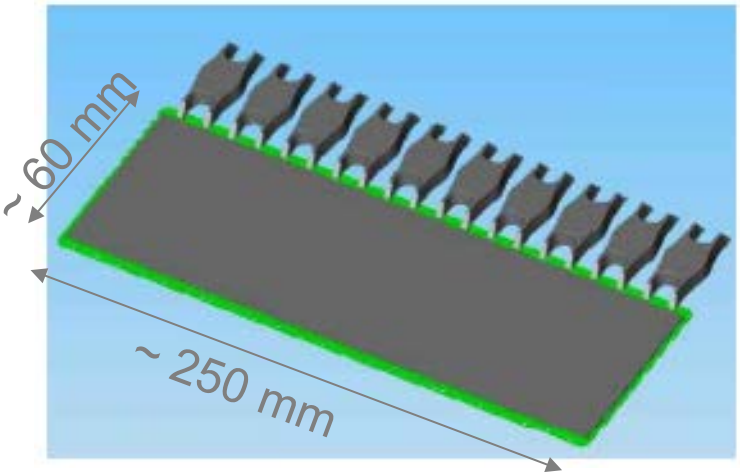
SiO_2-filled epoxy resin

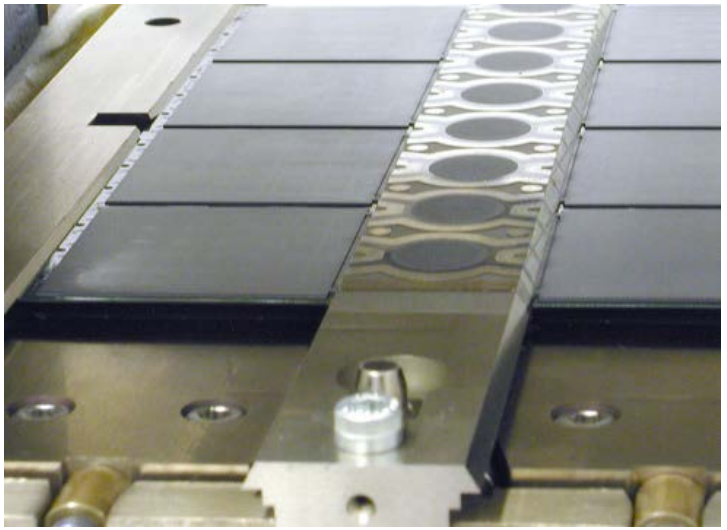
- Process Temp.: 160 – 180 °C
- Pressure: 50 - 150 bar
- Cycle Time: 1 - 2 min + 4h
- EMC: pellets
- Encapsulation: single & double sided
- Substrates: leadframe, PCB, DCB

Pin / Top Gate - Batchsize



Source: ASM





Source: Fico

Promising Technologies

What has to be packed in a PSiP (DC/DC converter)?

- Semiconductors (volume ~3%)
- Inductors -> ferrite (volume ~20%)
- Capacitors -> ceramics (volume ~10%)
- Conductors -> copper (~15%)
- Control, drivers, sensors (~12%)
- Insulation and unused volume (~40%)

-> especially the ceramic materials are a nightmare in thermomechanical properties

Promising Technologies

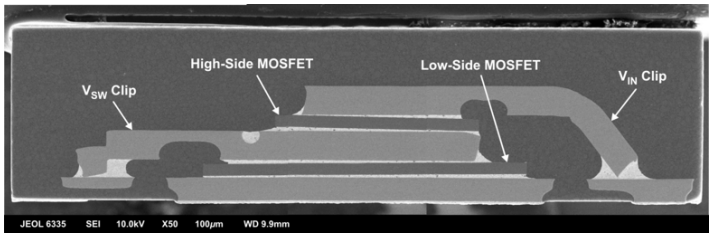
How to bring these different components together?

Electrical interconnect:

Solder Wire bond glued

sintered Galvanic copper Transient liquid phase bond

- Soldering is the only standardized technology, where all components are prepared for
- Galvanic copper is used in the PCB manufacturing process, if beneficial it can also be used for semiconductor interconnects
- Wire bonds are well established for semiconductors
- Sintering can be used for semiconductors



Cross section of a TI power stack with two chips soldered upon each other

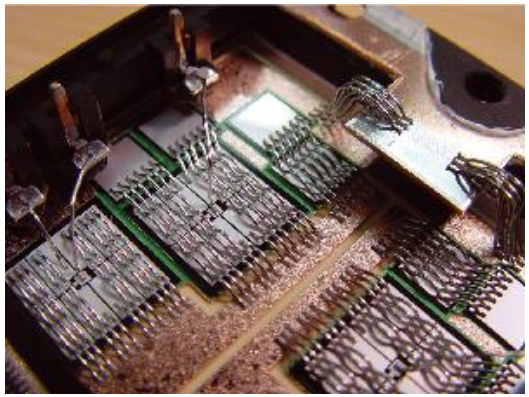
Promising Technologies

How to bring these different components together?

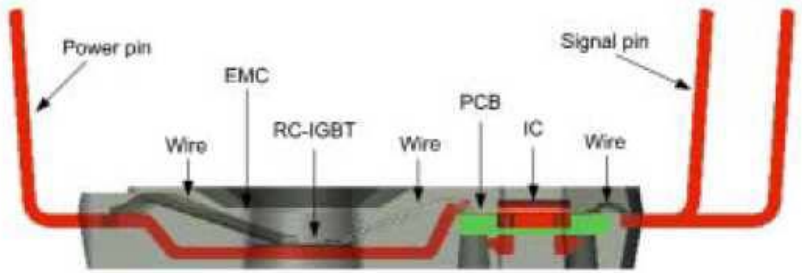
Substrate/carrier: PCB DCB LEAD FRAME

Insulated metal substrate

- PCB is allows a high complexity interconnects and additionally medium quality inductor windings
- Direct Copper Bond has the best thermal conductivity for a required insulation



- Lead frame is cheap but low complexity



Promising Technologies

How to bring these different components together?

Encapsulation: Transfer/Compression Mold

Plastic frame+Silicone

- Transfer Mold encapsulation enables robust *Systems in Package* and can improve reliability and thermal properties. Tooling and process ramp up is expensive
- Main advantage of plastic frame and silicone is flexibility for customized solutions

Promising Technologies

What are the promising technologies to **Power Systems in Package**?

- Carrying substrate and electrical interconnection: PCB
  higher number of interconnections compared to lead frame and wire bond, inductor manufacturing
  Future issues: *thermal performance*
- Electrical and mechanical component assembly: soldering
  all components are available for soldering, the variety of components requires an universal technology
- Encapsulation: Transfer/Compression mold
  enables environmental and handling protection, thermal improvement
  Future issues: *flexibility/package standardization*
- Chip interconnection: galvanic deposition in PCB process
  is already part of the production process, embedded chips safe space
  Future issues: *availability of copper metalized chips*

Resume

What are future research tasks?

- Optimizing power electronics development towards packaging requirements
- Building up experience on material and process knowledge to allow the integration of these heterogeneous components
- Qualifying the processes
- Identifying products with sufficient high production numbers to recover the development costs

-> a lot of work…