

Wafer Level System Integration

All Silicon System Integration Dresden - ASSID

FRAUNHOFER INSTITUTE FOR RELIABILITY AND MICROINTEGRATION IZM



3D SYSTEM INTEGRATION TSV INTERPOSER



Benefits:

- High performance
- High reliability
- High integration density
- High flexibility
- High yield

Technical features:

- High performance
- High reliability
- High integration density
- High flexibility
- High yield

Applications:

- High performance
- High reliability
- High integration density
- High flexibility
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Cu TSV INTEGRATION



Benefits:


- High performance
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Technical features:


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WAFER BUMPING ELECTROCHEMICAL DEPOSITION



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3D ASSEMBLY & STACKING



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WAFER SIMULATION / DICING



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DIRECT BONDING



Benefits:

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WAFER THINNING



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ADVANCED LITHOGRAPHY FOR 3D WAFER LEVEL SYSTEM INTEGRATION



Benefits:


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Technical features:


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METROLOGY



Benefits:

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ELECTRICAL WAFER LEVEL TEST



Benefits:

- High performance
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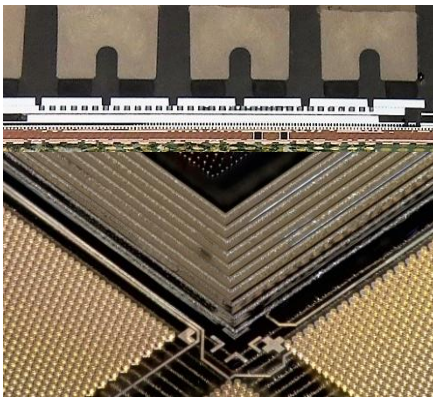
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IZM-ASSID is working with a certified management system to guarantee high quality standards.

3D SYSTEM INTEGRATION TSV INTERPOSER



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Silicon interposers with Through Silicon Vias (TSVs) are an important element for 3D system-in-packages (SiP) approaches. Main advantages of silicon interposers are the decoupling of front end and backend processing for the implementation of TSVs, redistribution layers (RDL) and the integration of active and passive devices. Interposer-based SiPs provide small form factors, excellent electrical properties, heterogeneous device integration, cost effective manufacturing and fast time-to-market.

TSV interposers are specified for various application areas which results also in different technical features ranging from high density TSV integration and high density RDL for digital applications to interposer for RF application as well as MEMS integration and optical interconnects.

Services for 300/200 mm wafers that are offered by Fraunhofer IZM according to industrial specifications include:

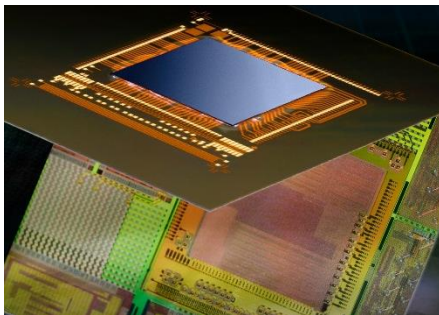
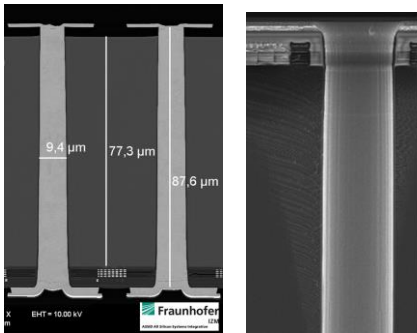
- Interposer SiP
- Customer specific design based on defined design guidelines
- Fabrication of high density silicon interposer with TSV and multi-layer redistribution
- Typical interposer features:
 - TSV diameter: 5/10/20 μm
 - TSV depth: > 100 μm
 - Cu-multilayer redistribution layer
- Integration of passive elements e.g. R, L, (C)
- Interconnect formation (micro bumps, Cu-Pillar, SnAg)
- Reliability assessment including thermo-mechanical and electrical characterization
- Prototyping, Low-Volume manufacturing



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Cu TSV INTEGRATION

Through Silicon Vias (TSV) are a key element for 3D wafer-level system integration. Fraunhofer IZM-ASSID has developed TSV processes (POR) for customer-specific applications, e. g. Via Middle, Via Last Back Side and Via Last Front Side. IZM-ASSID supports the evaluation and qualification of new materials for isolation, barrier / seed and TSV filling as well as the optimization of TSV post-processing (front side and back side). All processes are carried out using leading-edge, industry-compatible process equipment for 8" / 12" wafers.

Services for 300 (200) mm wafers that are offered by Fraunhofer IZM-ASSID include:

- Full Cu-TSV and Cu liner TSV integration in active CMOS device
- TSV process integration: via-last back side and front side / via-middle / via first
- Dry etch incl. wet cleaning: DRIE, RIE of Si and Dielectrics
- Isolation liner deposition: SATEOS, PETEOS, PESilan, PESiN
- Barrier/seed-layer deposition PVD: Ti, Ta, Cu, TiN, WTi and MOCVD: TiN, Co
- TSV metallization: Cu-ECD
- Metal anneal up to 400°C
- Front side / back side contact formation
- Basic design guidelines (diameter / depth):
 - min. 5 μm / 50 μm
 - typ. 10 μm / 120 μm
 - 20 μm / 120 μm
 - Back side TSV (Cu-liner) up to 250 – 700 μm depth

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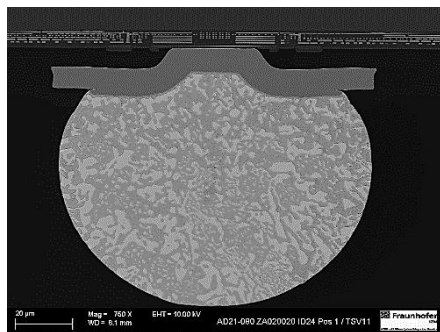
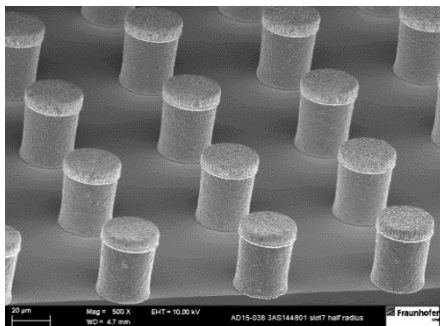


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WAFER BUMPING ELECTROCHEMICAL DEPOSITION



IZM provides qualified bumping services in silicon wafers (active/passive).

Micro bump structures of Cu, Cu-SnAg, SnAg, Cu-Ni-Au and Ni-Au are realized by electrochemical deposition with UBM metallization on 12" and 8" semi standard wafers. A fluxless reflow is used for solder bump reflow.

Services includes:

- Generation of mask design
- Application of photo polymer as protective layer
- Micro bumping on polymer ILD
- Micro bumping on I/O pad
- Copper bumping on polymer ILD
- Wafer dicing of bumped wafers
- Thinning of bumped wafers
- 2D/ 3D micro bump inspection (AOI) and mapping
- Material- and Equipment Evaluation

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Q4-21

μ-Bump Materials

Bump:	Cu / SnAg
	Cu pillar bump
Pad Metallization:	Cu / Ni / Au; Cu / Ni; Cu

Design Guide Lines

12" wafer
Customer specific bumping on request

Cu μ-Bump on Polymer

Polymer Via:	15 μm	35 μm
Bump Diameter:	15 μm	55 μm
Bump Pitch:	30 μm	100 μm
Bump Height:	25 μm	50 μm

Cu μ-Bump on I/O Al Pad

Bump Diameter:	typ. 25 μm
Bump Pitch:	min. 55 μm



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3D ASSEMBLY & STACKING

The following industrial services are offered by Fraunhofer IZM-ASSID:

Flip Chip Bonding

- Die-to-Wafer (D2W) Bonding
- Flux-activation or fluxless
- Dispensing Pre-applied underfill
- Inline or external reflow
- Die size: 3 – 30 mm
- Die thickness: $\geq 50 \mu\text{m}$
- Minimum pitch: $\geq 45 \mu\text{m}$
- Min. interconnect diameter: $\geq 25 \mu\text{m}$
- Placement accuracy: 3 – 10 μm @3sigma
- Die feed: 300mm Plastic Film Frame Carrier (Disco Type), WafflePack or GelPack (no Flip)

Vacuum Reflow

- Single wafer chamber
- Vacuum: 10⁻² / 10⁻³ mbar
- Anneal temperature: $\leq 450 \text{ }^\circ\text{C}$
- Temperature uniformity: $\pm 2 \text{ K}$
- Heating rate: $\geq 20 \text{ K/sec}$
- Cooling rate: $\leq 10 \text{ K/sec}$
- Purging and activation with nitrogen and formic acid
- free programmable gas flow, vacuum, process times and temperatures up to 50 steps

Flip Chip Underfill Dispensing

- Dispensing of various underfill materials
- Total needle placement accuracy: $\geq 50 \mu\text{m}$ @ 3sigma
- Different fluid pump systems (Line DU and Smart Stream)
- Edge Detection Vision Algorithm
- Automatic dispense mass calibration
- Height measurement sensor
- Substrate and needle heating
- Automatic needle cleaning and detection
- Maximum sample size (LxWxH): 300x300x50

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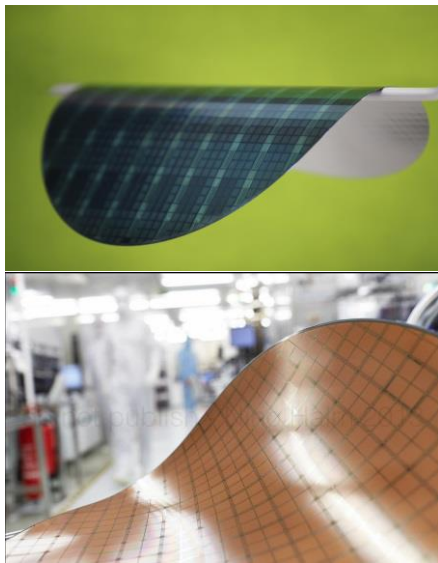
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WAFER THINNING

Fraunhofer IZM-ASSID offers services for wafer thinning (8"-12") based on grinding and polishing with and without topography e.g. bumped wafers.

Back Grinding Tape Lamination

- Back Grinding (BG) Tape Lamination of 300 (200) mm UV and Non-UV tapes

Wafer Backgrinding

- Back grinding technologies:
 - Grinding Before Dicing (GBD)
 - Dicing before Grinding (DBG)
 - 300 mm TAIKO Grinding
- Wafer Backgrinding/Polish of 300 (200) mm single wafers
 - Rough grinding: mesh 320, mesh 600
 - Fine grinding: mesh 1500, mesh 4000, mesh 6000
 - Dry polish: Ra 0.0003µm, Ry = 0.0017µm
 - Stress relief etch: SF6 or CF4 based
 - Incoming wafer thickness: ≥ 500µm
 - Outgoing wafer thickness: ≥ 50µm
 - TTV: ≤ 5µm pending on wafer frontside topology
- Wafer Backgrinding/Polish of 300 (200)mm temporary bonded wafer stacks

- Rough grinding: mesh 320, mesh 600
- Fine grinding: mesh 1500, mesh 4000, mesh 6000
- Dry polish: Ra 0.0003µm, Ry = 0.0017µm
- Stress relief etch: SF6 or CF4 based
- Incoming wafer thickness: 700 – 1600µm
- Outgoing device wafer thickness: ≥ 20µm
- TTV: ≤ 5µm pending on incoming topology of application

Wafer Mounting, Peeling, Exposure

- Inline wafer mounting and BG tape peeling of 300 (200) mm single wafers on 300 (200) mm Film Frame Carrier (Disco type, metal or plastic film frame carrier)
- Application of various UV- and Non-UV dicing tapes including DAF-tape
- Inline exposure of UV-tapes
- Packing and transportation of Film Frame Carrier in 300 (200) mm Film Frame Shipper



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WAFER SINGULATION / DICING

The following industrial services are offered by Fraunhofer IZM-ASSID:

Wafer Singulation - Mechanical Blade Dicing

- Mechanical blade dicing of 300 (200) mm single wafer (50 – 775µm thickness)
- Dicing technologies: Single Cut (Dual Cut), Step Cut, Half Cut (Dual Cut)
 - Grid type: SD
 - Grid size: mesh 1700 – 3500 (pending on blade type)
 - Kerf width: 0,025 – 0,06mm (pending on blade types)
 - Exposure height: 0,38 – 1,24mm (pending on blade type)

Wafer Singulation - Laser Grooving

LATEST GENERATION OF ps LASER GROOVER (DISCO corp)

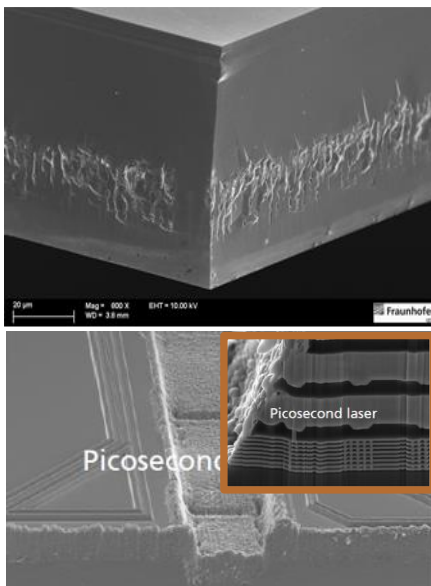
- Dicing technology: Ultra-Fast pico-second Laser
 - Spin coating of surface protection film before laser grooving
 - Inline analysis of coating quality before grooving
 - Grooving of lowk/ ultra-lowk materials and BEOL metallization in dicing street with minimal recast and straight and properly sealed groove walls
 - Laser full cut of ultra thin dies ($\leq 50\mu\text{m}$)
 - Cleaning wafer surface from protection film

Wafer Singulation - Laser Stealth Dicing

- Dicing technology: High throughput laser engine for silicon singulation (dry process)
 - Applicable to higher doped wafers ($> 0,02 \text{ Ohm}\cdot\text{cm}$)
 - IR- camera allows wafer recognition also from back side
 - Applicable to ultra-thin wafer, single standard wafer, compound wafer
 - Applicable for sample preparation in physical failure analysis (extremely shorten preparation time in cross-sectioning)
 - Wafer expansion and Remounting

Wafer Edge Trimming

- Grid type: SD
- Grid size: mesh 1700 – 2000 (pending on blade type)
- Kerf width: 0,5 – 1mm (pending on blade types)



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ELECTRICAL WAFER LEVEL TEST

The following industrial services are offered by Fraunhofer IZM-ASSID:

Fully Automated Wafer Testing

- Advantest CTH 93000 Platform
 - 128 ch Digital Test capability PS1600
 - 128 ch DPS capability AVI64
 - 8 ch High Power Test capability PVI8
 - Upgradeable for customer specific applications
- TEL Precio Platform
 - 300mm (200mm capable)
 - wafer thickness 300-1600µm
 - Wafer bow up to 1.5mm
 - Dual loader configuration
 - 12" Probecard Pogo Tower Interface with SACC
 - Chuck cooling and heating range -55°C/-40°C up to 150°C/200°C
 - RF shielded and lightproof measurement chamber
- Testprogram development for functional tests in cooperation with partners
- Automated Dataprocessing with classification, Bin Map, Merging Bin Maps



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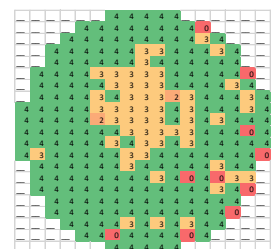
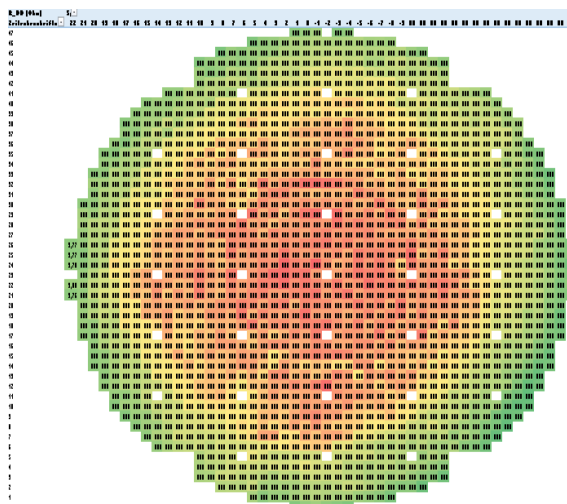
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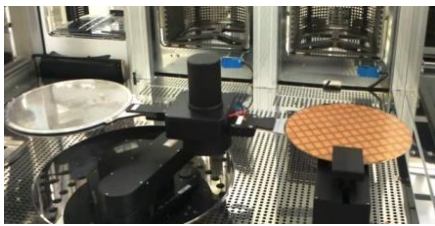
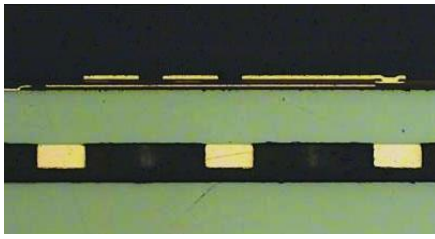
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TEMPORARY WAFER BONDING / DEBONDING

Fraunhofer IZM-ASSID offers service for temporary wafer bonding /debonding (8"/12" wafers) and permanent wafer bonding (8"/12" wafers)

Temporary Wafer Bonding

Wafer diameter: 300 (200) mm

- Coating and pre-baking of various wafer bond adhesives
- Bonding forces: 100N up to 60kN (programmable profiles)
- Process vacuum: $\leq 1 \cdot 10^{-5}$ mbar
- Process temperatures: $\leq 550^{\circ}\text{C}$ with programmable profiles

Wafer Debonding

- Wafer diameter: 300 (200)mm
- Slide-off debonding with temperatures up to 350°C
- EdgeZone-Release debonding at room temperature
- Thin wafer handling down to $100 \mu\text{m}$ thickness
- Wafer flipping capability
- Wafer cleaning after de-bonding with different adhesive solvents
- Wafer mounting on film frame carrier

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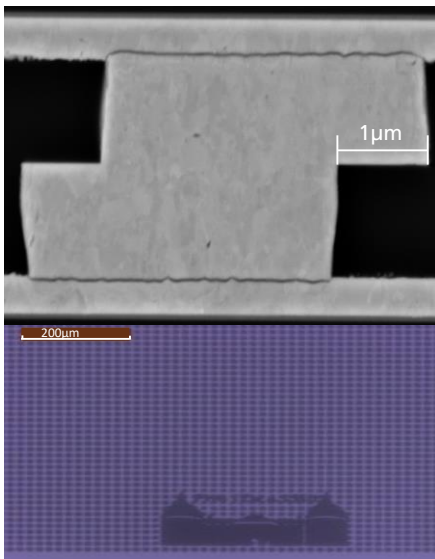
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DIRECT BONDING

Direct Oxide to Oxide Bonding (ZiBond®)

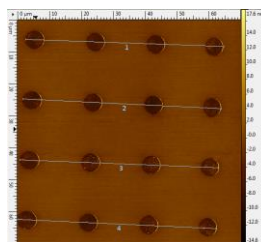
- Wafer diameter: 300 mm
- Technology is jointly developed by Xperi and IZM ASSID
- ZiBond® is a low temperature homogeneous (e.g. oxide-to-oxide) direct bonding technology that forms strong bonds between wafers or die with same or different coefficients of thermal expansion (CTE).
- Wafer level bonding is performed at room temperature in less than a minute, followed by low temperature batch annealing to strengthen the bond

Direct Oxide-Oxide and Cu-Cu Bonding (DBI Bond®)

- Wafer diameter: 300 mm
- Technology is jointly developed by Xperi and IZM ASSID
- DBI is an extension of Ziptronix' ZiBond technology that allows an interconnect pitch of less than 10 microns, and accommodates 1.5 million connections per square centimeter.
- The process uses standard fab tools to planarize the wafer surface and introduce a thin layer of silicon dioxide, which allows hermetic bonding at low temperatures (300 °C).
- alignment accuracy: $\pm 1 \mu\text{m}$

Benefits of Direct Bonding

- ✓ *Fine pitch 3D interconnect:* Scales from 40 μm to 1 μm or less
- ✓ *High Bandwidth:* Enables increase in I/O as needed
- ✓ *Improved Performance:* elimination of micro bumps, underfill and solder enhances electrical and thermal characteristics
- ✓ *Yield improvement:* minimizes warpage during assembly
- ✓ *Low cost:* reduces process steps and simplifies manufacturing process



Fraunhofer Testchip

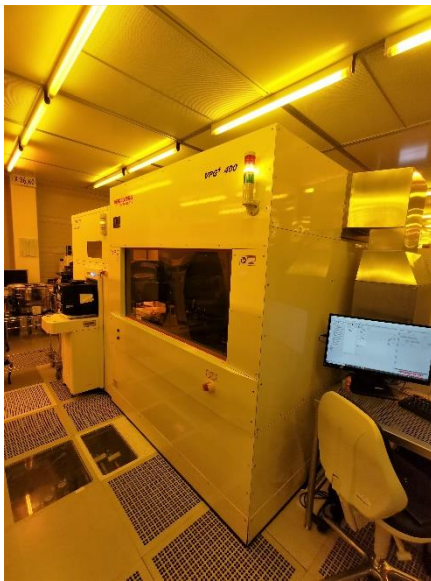
- 18 μm pad pitch
- Metal density: 4.5 %



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ADVANCED LITHOGRAPHY FOR 3D WAFER-LEVEL SYSTEM INTEGRATION

Fraunhofer IZM-ASSID offers advanced lithography capabilities for Wafer-Level System Integration

- Full area maskless exposure system
- Fully automated FOUP to FOUP processing for 8" and 12" wafer
- Handling system for Si wafer, glass wafer, stacked wafer, warped wafer
- Multiple write modes
- Camera system for layer alignment and metrology (CD, overlay)
- Real time auto focus system
- Multiple alignment modes for 3D integration
- Gray scale lithography exposure mode
- Perfect solution for rapid prototyping
- Excellent R&D alternative to mask based exposure systems
- Specialized for applications that require high precision microstructures: Advanced Packaging, 3D system integration, microfluidics, MEMS, BioMEMS, and compound semiconductors

Technical specification exposure module

- Minimum feature size: 750 nm
- Top side alignment accuracy down to 100 nm
- Multiple alignment modes for front-to-back-side with <math><1\mu\text{m}</math> accuracy

Write Mode	I	II	III	IV
Minimum structure size [μm]	0.75	1	2	4
Address grid [nm]	12.5	25	50	100
Edge roughness [3σ , nm]	40	50	70	150
CD uniformity [3σ , nm]	65	75	110	300
2nd layer alignment [3σ , nm]	100	150	225	300

Fraunhofer Institute for Reliability and Microintegration IZM

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IZM-ASSID is working with a certified management system to guarantee high quality standards.

METROLOGY

The focus in Focus at IZM-ASSID are investigations of 3D-Features e.g.:

- high speed bump height measurements
- high accurate TSV-depth measurements
- layer (thickness and profile) in reference to process flow
- 3D failure characterization for hidden structures (e.g. TSV-copper fill; interconnects of multi die stacks)

The following metrology services are offered by Fraunhofer IZM-ASSID:

Bump Height Measurement

- white light triangulation
 - bump height 7-80 μm
 - up to 25 million bumps per wafer
- high throughput measurement (max. 15 wph)
- automated 4" - 12" wafer handling

TSV-depth Measurement

- interferometric depth measurement
 - 1 μm up to 300 (confocal: 700 μm)
- up to 12" wafer

Defect Inspection

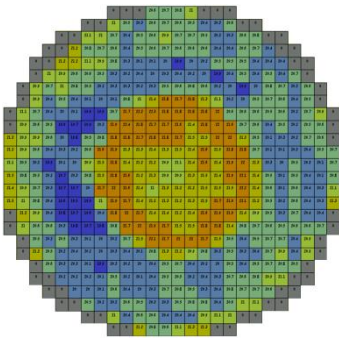
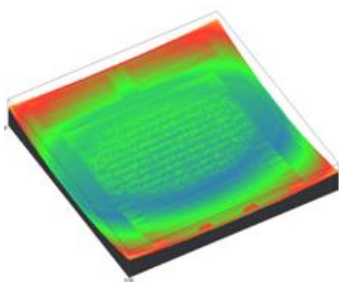
- automated defect inspection (AOI)
 - min. defect size 1 μm -5 μm (depends on structure complexity and contrast)
- automated 4" - 12" wafer handling & film frames

Topology

- confocal microscopy
 - 5 nm surface topology @ mag 20x (opaque materials: higher accuracy)
- up to 12" wafer

Layer Thickness

- ellipsometry (thin layers):
 - 5-2000 nm Oxid / 5-150 nm Nitrid
 - polymer <5 μm
 - layer stack with up to 3 layers
- interferometric layer thickness measurement (thick layers):



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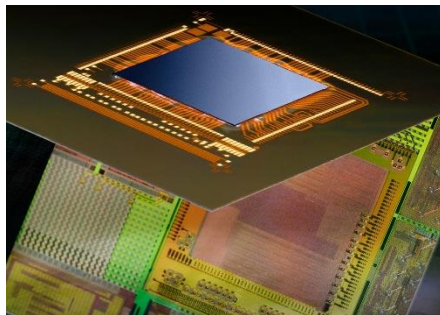
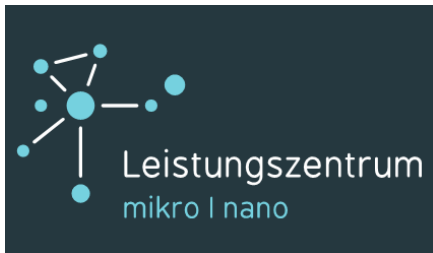
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MoHeSys

High Performance Center Micro-Nano-Electronics Dresden



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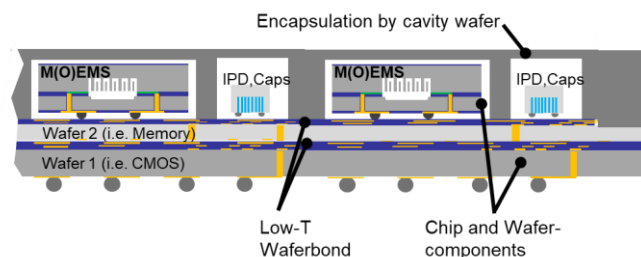
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- Modular wafer level packaging technologies for flexible and rigid encapsulated sensor systems
- Applications: Wearables. Light weight structures, flexible electronics, smart cards
- Project focus:
 - Component miniaturization
 - System integration
 - Reliability assessment
- Planned demonstrators:

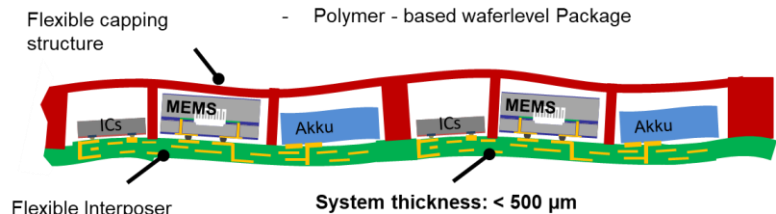
Multi-Wafer-System

- Rigid wafer level stack
- Target application: High Performance computing



Flexible Interposer

- Ultra thin / flexible structure
- Polymer - based waferlevel Package



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